NM9A02G08 NAND Flash Memory Datasheet

3.3V, x8 2G-BIT NAND Flash

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- **Memory Cell Array Organization (with spare)**
  - Page size: 2112 bytes (2048 + 64 bytes)
  - Block size: 64 pages (128K + 4K bytes)
  - Plane size: 2 planes X 1024 blocks per plane
  - Device size: 2048 blocks = 2Gbit
- **I/O Performance**
  - Page Read: 25us Max without internal ECC
    70us Max with internal ECC
  - Page Program: 600us Max (with or without internal ECC)
- **Internal Data Move**
  - Fast data copy without external buffering
- **Cache Program**
  - Improves program throughput with internal buffer
- **Read Cache**
  - Improves read throughput
- **Fast Block Erase**
  - Block erase time: 0.7ms Typ, 3ms Max
- **Electronic Signature**
  - ONFI Signature
  - Unique ID
- **Status Register**
- **Data Integrity**
  - Data retention: 10 years
  - Endurance: 100K Program / Erase cycles
- **Operating Temperature Range**
  - -40℃ to 85℃
- **Package**
  - FBGA63

2. General Description

The NeuMem NM9A02G08 is a 2Gbit Parallel NAND Flash device with internal ECC that complies with ONFI 1.0 specification. The device includes industry-standard features, which provides cost-effective solution for applications requiring high-density, solid-sate storage. The device is a single-die package. It employs a multiplexed 8-bit bus (IO[7:0]) to convey command, address and data, and the bus interface protocol is controlled by signals: ALE, CE#, CLE, RE# and WE#. Additional signals implementing block lock (LOCK), hardware write protection (WP#) and device status monitor (R/B#) are also available.

The device has a traditional NAND interface that does not include a clock signal. It uses RE# to latch data read, and WE# to latch data written. Commands, Addresses and Data are asynchronously introduced using the control pins.

Program operation is done on a page basis; each page of data can be programmed in tPROG (internal ECC disabled) or tPROG_ECC (internal ECC enabled). Erase operation is done on each block, and a block is erased in tBERS. An on-chip controller automates program and erase operations by performing required internal tasks.

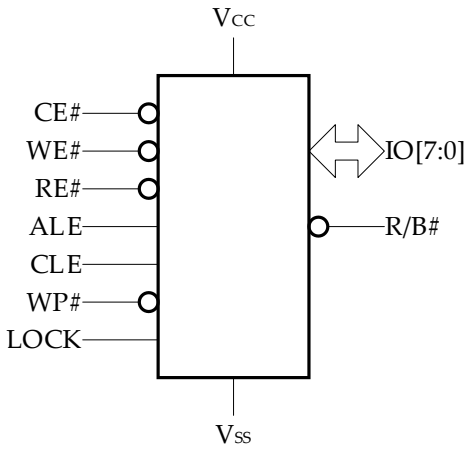

Figure 1: Logic Diagram

2.1. Product List

Table 1: Product List

Part Number	Device Interface	Vcc	Package
NM9A02G08AFI	x8 bit	3.3V	FBGA63

2.2. Pin Description

A full description of all pins of the device is offered in the following table.

Table 2: Pin Definitions

Signal	Direction	Description
ALE	Input	**Address Latch Enable** When ALE is High, it indicates an address bus cycle.
CE#	Input	**Chip Enable** The CE# active-low input selects the device. When CE# is high and the device is in Ready state, the device goes into standby mode.
CLE	Input	**Command Latch Enable** When CLE is High, it indicates a command bus cycle.
LOCK	Input	**Block Lock.** The Block Lock function is enabled if LOCK pin is 1 while the device is power up. The function is disabled if LOCK is 0 or unconnected during power up. This pin has internal pull-down resistor.
RE#	Input	**Read Enable True** The falling edge of RE# drives internal data to the IO[7:0] bus.

WE#	Input	**Write Enable** Data, command and address are latched on the rising edge of WE#.
WP#	Input	**Write Protect** The WP# active-low input disables Flash array PROGRAM and ERASE operations.
IO[7:0]	I/O	**Data Inputs/Outputs** The 8-bit-wide bidirectional I/O bus conveys command, address and data to and from the device.
R/B#	Output	**Ready/Busy** The R/B# pin is an open drain output that requires an external pull-up. This signal indicates the device status. When R/B# is low, it indicates that one or more LUN operations are in progress.
Vcc	Supply	**Power Supply** Power supply for the device.
Vss	Supply	**Ground** Power supply ground.
NC	-	**No Internal Connection** A NC pin has no internal connection; it can be either unconnected or driven.
DNU	-	**Do Not Use** A DNU pin should be unconnected.

2.3. Block Diagram

The device uses NAND Flash cell array to store data. Device operations are implemented through a series of internal registers. A block diagram of the device is shown below.

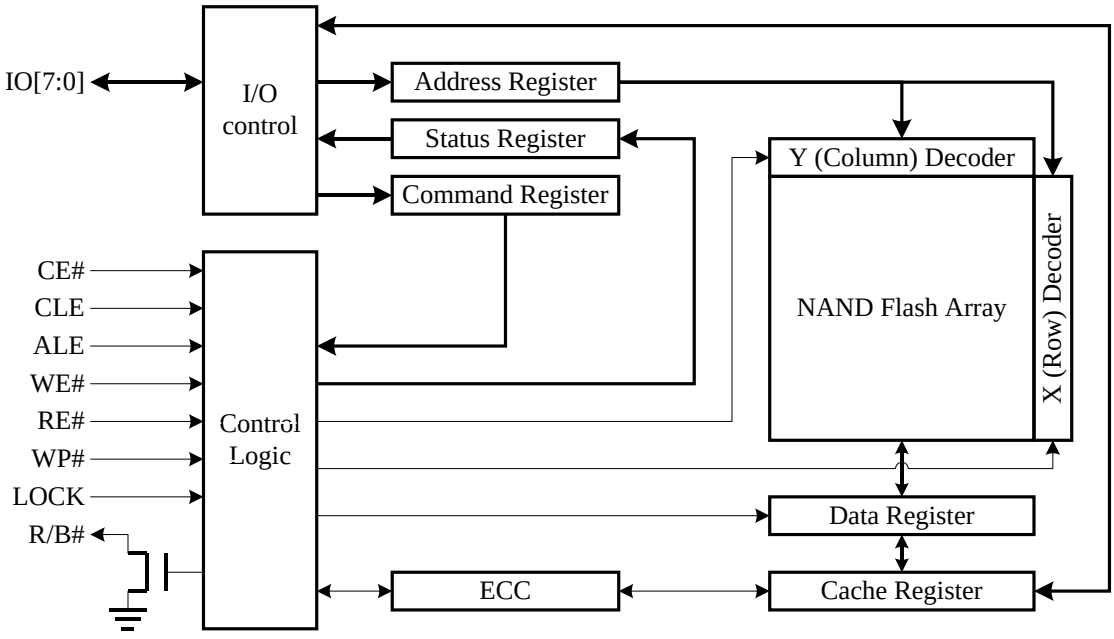

Figure 2: NAND Flash Block Diagram

2.4. Memory Organization

The device memory array is organized in descending hierarchical order: plane, block, page and column. Data is programmed and read in page-based operations, and erase operations shall occur in a block-based manner.
The devices are erased upon delivery. Due to device physics limitations, any programmed page address in the

device is not eligible for another program operation and it has to be explicitly erased to make it available for upcoming program operations.

The memory organization is shown in the following figure.

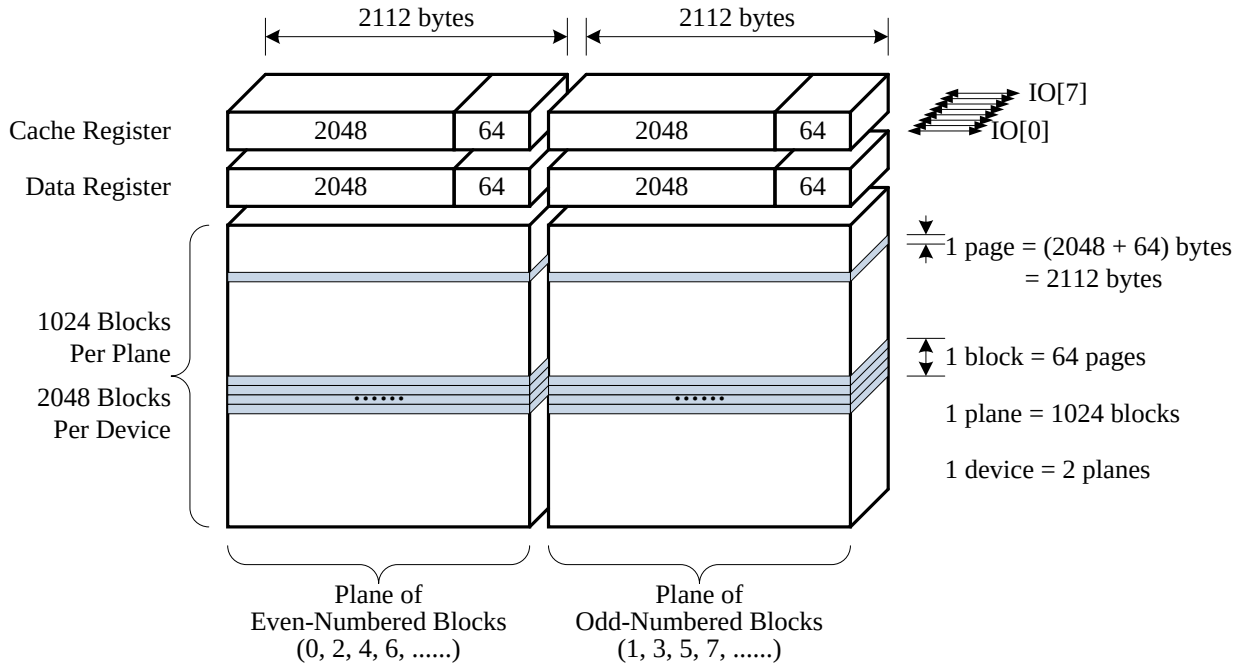

Figure 3: Array Organization

2.5. Array Addressing

The device memory array addressing is defined as follows.

Table 3: Memory Array Addressing

Bus Cycle	IO[7]	IO[6]	IO[5]	IO[4]	IO[3]	IO[2]	IO[1]	IO[0]
1st Cycle	CA[7]	CA[6]	CA[5]	CA[4]	CA[3]	CA[2]	CA[1]	CA[0]
2nd Cycle	Low	Low	Low	Low	CA[11]	CA[10]	CA[9]	CA[8]
3rd Cycle	BA[7]	BA[6]	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]
4th Cycle	BA[15]	BA[14]	BA[13]	BA[12]	BA[11]	BA[10]	BA[9]	BA[8]
5th Cycle	Low	Low	Low	Low	Low	Low	Low	BA[16]

Notes:

1. BA = Block Address, PA = Page Address, CA = Column Address.
2. Actual page address = BA + PA.
3. If CA[11]=1, then CA[10:6] should be all 0s.
4. BA[6] is for plane selection.

2.6. Command Set

All commands supported by the device are defined in the following table.

Table 4: Command Set

Command	1st Cmd Cycle	Address Cycles	Data Input Cycles	2nd Cmd Cycle	Valid When Selected LUN Busy	Valid When Other LUN Busy
Reset	FFh	0	-	-	Yes	Yes
Read ID	90h	1	-	-	No	No
Read Parameter Page	ECh	1	-	-	No	No

Read Unique ID	EDh	1	-	-	No	No
Get Features	EEh	1	-	-	No	No
Set Features	EFh	1	4	-	No	No
Read Status	70h	0	-	-	Yes	
Read Status Enhanced	78h	3	-	-	Yes	Yes
Random Data Read	05h	2	-	E0h	No	Yes
Random Data Input	85h	2	Optional	-	No	Yes
Program For Internal Data Move	85h	5	Optional	-	No	Yes
Read Mode	00h	0	-	-	No	Yes
Read Page	00h	5	-	30h	No	Yes
Read Page Cache Sequential	31h	0	-	-	No	Yes
Read Page Cache Random	00h	5	-	31h	No	Yes
Read Page Cache Last	3Fh	0	-	-	No	Yes
Program Page	80h	5	Yes	10h	No	Yes
Program Page Cache	80h	5	Yes	15h	No	Yes
Erase Block	60h	3	-	D0h	No	Yes
Read For Internal Data Move	00h	5	-	35h	No	Yes
Program For Internal Data Move	85h	5	Optional	10h	No	Yes
Block Unlock Low	23h	3	-	-	No	Yes
Block Unlock High	24h	3	-	-	No	Yes
Block Lock	2Ah	-	-	-	No	Yes
Block Lock-Tight	2Ch	-	-	-	No	Yes
Block Lock Read Status	7Ah	3	-	-	No	Yes
OTP Data Lock By Page (ONFI)	80h	5	No	10h	No	No
OTP Data Program (ONFI)	80h	5	Yes	10h	No	No
OTP Data Read (ONFI)	00h	5	No	30h	No	No

Notes:

1. Busy is denoted by RDY bit in Status Register being 0.
2. If a command is valid when other LUNs are busy, it means the command is used in interleaved die operations.
3. For Read For internal Data Move and Program For Internal Data Move commands, the operation should stay within plane address boundaries.
4. Read Page Cache Sequential, Read Page Cache Random, Read Page Cache Last and Program Page Cache commands are available only when internal ECC is disabled.
5. If the previous command is Read Page (00h-30h) or Read Page Cache series command, then a Read Page Cache series command (31h, 00h-31h, 3Fh) while the array is busy (RDY=1, ARDY=0) is supported. Otherwise, it is prohibited.
6. If the previous command is Program Page Cache (80h-15h) command, then a Program Page Cavhe (80h-15h) command while the array is busy (RDY=1, ARDY=0) is supported. Otherwise, it is prohibited.
7. OTP commands must be placed behind Set Features command with appropriate feature address.

Table 5: Two-Plane Command Set

Command	1st Cmd Cycle	Address Cycles	2nd Cmd Cycle	Address Cycles	3nd Cmd Cycle	Valid When Selected LUN Busy	Valid When Other LUN Busy
Read Page Two-Plane	00h	5	00h	5	30h	No	Yes

Read For Two-Plane Internal Data Move	00h	5	00h	5	35h	No	Yes
Random Data Read Two-Plane	06h	5	E0h	-	-	No	Yes
Program Page Two-Plane	80h	5	11h-80h	5	10h	No	Yes
Program Page Cache Mode Two-Plane	80h	5	11h-80h	5	15h	No	Yes
Program For Two-Plane Internal Data Move	85h	5	11h-85h	5	10h	No	Yes
Block Erase Two-Plane	60h	3	D1h-60h	-	D0h	No	Yes

Notes:

1. Read For Internal Data Move Two-Plane and Program For Two-Plane Internal Data Move commands should stay within plane boundaries.
2. Random Data Read Two-Plane command can only be used with Page Read Two-Plane command.
3. For Block Erase Two-Plane command, D1h is not necessary and can be omitted.
4. Two-Plane commands are available only when internal ECC is disabled.

2.7. OTP Pages

This NAND Flash device contains a one-time-programmable (OTP) area in the LUN, which totally has 30 pages with 2112 bytes in each page. The page address of OTP area ranges from 02h, 03h, 04h through to 1Fh. All OTP pages are guaranteed to be good.

The device is shipped from the factory with all OTP bits being 1. Programming and partial-page programming operations can convert OTP bits from 1 to 0, but once it becomes 0 it can never return to 1. Erase operations have no effect in OTP area, regardless of its protect status. The user may also choose to protect the OTP area to prevent any further programming operations.

OTP operations can be accomplished only when the device is in OTP mode. By setting specific feature bits using Set Features (EFh) commands, the user can enter or exit OTP mode. The user may also acquire OTP status using Get Features (EEh) commands.

2.8. Legacy OTP Commands

For compatibility reasons, the device supports OTP Data Program (A0h-10h), OTP Data Protect (A5h-10h) and OTP Data Read (AFh-30h) commands.

2.9. Device Feature Table

Devices are shipped with a feature table inside of the memory array, which is available for the host to determine the current settings of the device. The feature table can be read or modified via the Get Feature or Set Feature commands. Feature information is stored into multiple addresses, as is defined in the following table.

Table 6: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing Mode
02h - 7Fh	Reserved
80h	Programmable I/O Drive Strength
81h	Programmable R/B# Pull Down Strength
82h - FFh	Reserved

90h	Array Operation Mode

2.9.1.Feature Address 01h: Timing Mode

The definition of Timing Mode feature at address 01h is given below.

Table 7: Feature Address 01h: Timing Mode

Subfeature Parameter	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	Reserved (0)					Timing Mode Number		
P2	Reserved (00h)							
P3	Reserved (00h)							
P4	Reserved (00h)							

Notes:

1. Reserved: Reserved values are zero by default.
2. This feature address determines the maximum speed of the device.
3. The device is in the default Mode 0 upon power-up.
4. Timing Mode Number:
   Mode 0 = 000 (default)
   Mode 1 = 001
   Mode 2 = 010
   Mode 3 = 011
   Mode 4 = 100
   Mode 5 = 101
5. Modes 0 through 4 apply to 1.8V and 3.3V operations.
6. Mode 5 only applies to 3.3V operations.

2.9.2.Feature Address 80h: Programmable I/O Drive Strength

The device I/O drive strength setting can be selected at Feature Address 80h.

Table 8: Feature Address 80h: I/O Drive Strength

Subfeature Parameter	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	Reserved (0)						I/O Drive Strength	
P2	Reserved (00h)							
P3	Reserved (00h)							
P4	Reserved (00h)							

Notes:

1. Reserved: Reserved values are zero by default.
2. This feature address determines the device I/O drive strength, which should be selected based on the bus loading.
3. The device is in full strength upon power-up.
4. I/O Drive Strength:
   Full = 00b (default)
   Three-quarters = 01b
   One-half = 10b
   One-quarter = 11b

2.9.3.Feature Address 81h: Programmable R/B# Pull-Down Strength

The pull-down strength at R/B# pin of the device can be selected at Feature Address 81h.

Table 9: Feature Address 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	Reserved (0)						R/B# Pull-Down Strength	
P2	Reserved (00h)							
P3	Reserved (00h)							
P4	Reserved (00h)							

Notes:

1. Reserved: Reserved values are zero by default.
2. This feature address determines the R/B# pull-down strength, which should be selected based on the loading of R/B# pin.
3. The device is in full strength upon power-up.
4. R/B# Pull-Down Strength:
   Full = 00b (default)
   Three-quarters = 01b
   One-half = 10b
   One-quarter = 11b

2.9.4.Feature Address 90h: Array Operation Mode

Feature address 90h determines the operation mode of the device.

Table 10: Feature Address 90h – OTP Mode

Subfeature Parameter	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	Reserved (0)				Operation Mode			
P2	Reserved (00h)							
P3	Reserved (00h)							
P4	Reserved (00h)							

Notes:

1. Reserved: Reserved values are zero by default.
2. The operation mode bits are reset to 0s upon power-up.
3. Operation Mode in terms of OTP operation:
   Normal = 0000b
   OTP operation = 0001b
   OTP protection = 0011b
4. Operation Mode in terms of internal ECC:
   Disable ECC = 0000b
   Enable ECC = 1000b

2.10. Device ID

The NAND Flash devices are shipped with identification codes to provide information on device type, manufacturer ID, device configurations, etc.

2.10.1. ID: Address 00h

Device ID at address 00h provides device specific information including manufacturer code, device identifier, flash array cell type, page size, among many other device configurations.

Table 11: Device ID: Manufacturer ID (Address = 00h)

#	Parameter	Options	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	Value
Byte 0	JEDEC Manufacturer ID	NeuMem	0	0	1	0	1	1	0	0	2Ch
Byte 1	Device ID	NM9A02G08AFI	1	1	0	1	1	0	1	0	DAh
Byte 2	Number of die per CE	1							0	0	00b
	Cell type	SLC					0	0			00b
	Number of simultaneously programmed pages	2			0	1					01b
	Interleaved operations between multiple die	Not Supported		0							0b
	Cache programming	Supported	1								1b
	Byte Value	NM9A02G08AFI	1	0	0	1	0	0	0	0	90h
Byte 3	Page size	2KB							0	1	01b
	Spare area size (bytes)	64B						1			1b
	Block size (without spare)	128KB			0	1					01b
	Organization	x8		0							0b
		x16		1							1b
	Serial access (MIN)	1.8V: 25ns	0				0				0xxx0b
		3.3V: 20ns	1				0				1xxx0b
	Byte Value	NM9A02G08AFI	1	0	0	1	0	1	0	1	95h
Byte 4	ECC level	4-bit ECC / 512 (main) + 4 (spare) + 8 (parity) bytes							1	0	10b
	Planes per CE#	2					0	1			01b
	Plane size	1Gb		0	0	0					000b
	Internal ECC	ECC disabled	0								0b
		ECC enabled	1								1b
	Byte Value	NM9A02G08AFI	0	0	0	0	0	1	1	0	06h

2.10.2. ID: Address 20h (ONFI Signature)

Command 90h in combination with an address of 20h retrieves ONFI signature from the device, indicating that the device supports ONFI specification.

The ONFI signature is the ASCII encoding of "ONFI" where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h.

Table 12: Device ID: ONFI Signature (Address = 20h)

#	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	Value
Byte 0	"O"	0	1	0	0	1	1	1	1	4Fh
Byte 1	"N"	0	1	0	0	1	1	1	0	4Eh
Byte 2	"F"	0	1	0	0	0	1	1	0	46h

#	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	Value
Byte 3	"I"	0	1	0	0	1	0	0	1	49h
Byte 4	Undefined	X	X	X	X	X	X	X	X	XXh

2.11. Parameter Page

Parameter page is a data structure that describes the device's organization, features, timings and other behavioral parameters, offering a means to provide the host with sufficient information necessary to successfully communicate with the NAND Flash device.

The following table defines the parameter page data structure. To ensure the reliability of parameter data storage, x8 devices contain at least eight copies of the parameter page, and x16 devices contain at least four copies. If CRC checking indicates an incorrect copy is retrieved by the initial Read Parameter Page (ECh) command, the command can be resent to the device until a valid copy is available.

Table 13: Parameter Page Definition

Byte	Description		Value
0-3	Parameter page signature: 4Fh is ASCII for "O"; 4Eh is ASCII for "N"; 46h is ASCII for "F"; 49h is ASCII for "I".		4Fh, 4Eh, 46h, 49h
4-5	Revision number		02h, 00h
6-7	Features supported	NM9A02G08AFI	18h, 00h
8-9	Optional commands supported		3Fh, 00h
10-31	Reserved.		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32-43	Device manufacturer		4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44-63	Device model	NM9A02G08AFI	4Dh, 54h, 32h, 39h, 46h, 32h, 47h, 30h, 38h, 41h, 42h, 41h, 45h, 41h, 48h, 34h, 20h, 20h, 20h, 20h
64	Manufacturer ID		2Ch
65-66	Date code.		00h, 00h
67-79	Reserved.		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80-83	Number of data bytes per page.		00h, 08h, 00h, 00h
84-85	Number of spare bytes per page.		40h, 00h
86-89	Number of data bytes per partial page.		00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page.		10h, 00h
92-95	Number of pages per block.		40h, 00h, 00h, 00h
96-99	Number of blocks per logical unit.		00h, 08h, 00h, 00h
100	Number of logical units.		01h
101	Number of address cycles.		23h
102	Number of bits per cell.		01h
103-104	Bad blocks maximum per unit.		28h, 00h
105-106	Block endurance.		01h, 05h

Byte	Description		Value
107	Guaranteed valid blocks at beginning of target.		01h
108-109	Block endurance for guaranteed valid blocks.		00h, 00h
110	Number of programs per page.		04h
111	Partial programming attributes.		00h
112	Number of bits ECC correctability.		04h
113	Number of interleaved address bits.		01h
114	Interleaved operation attributes.		0Eh
115-127	Reserved.		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O pin capacitance.		0Ah
129-130	Timing mode support	NM9A02G08AFI	3Fh, 00h
131-132	Program cache timing mode support.	NM9A02G08AFI	3Fh, 00h
133-134	tPROG Maximum page program time.		58h, 02h
135-136	tBERS Maximum block erase time.		B8h, 0Bh
137-138	tR Maximum page read time.		19h, 00h
139-140	tCCS Minimum.		64h, 00h
141-163	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164-165	Vendor-specific revision number.		01h, 00h
166-253	Vendor-specific.		01h, 00h, 00h, 02h, 04h, 80h, 01h, 81h, 04h, 01h, 02h, 01h,0Ah, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h,00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h,00h, 00h, 00h, 00h(
254-255	Integrity CRC.		Set during test.
256–511	Value of bytes 0–255.		
512–767	Value of bytes 0–255.		
768+	Additional redundant parameter pages.		

2.12. Unique ID

The device comes with a Unique ID feature to allow for the implementation of serial number mechanisms which the user may leverage for security considerations. A combination of Unique ID and device manufacturer is truly unique.

The device has sixteen copies of unique ID in its internal memory array, each copy being 32 bytes in length. Within each copy, the first 16 bytes are the unique data, with the second 16 bytes being its complement, which enables the host designer to utilize XOR operation to check data integrity. Should the XOR data check fail, the

host can repeat the XOR operations on subsequent copies until a correct copy is detected.

Table 14: Unique ID and Its Complement

Bytes	Value
0-15	Unique ID
16-31	Unique ID's bit-wise complement

2.13. Status Register

The Status Register offers a means for the host to poll the status of the previous operation. The host can launch either Read Status or Read Status Enhanced operations to retrieve Status Register value from the device.
The status register is defined as below.

Table 15: Status Register Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Description
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	0 = Protected 1 = Not protected
6	RDY	RDY cache	RDY	RDY cache	RDY	0 = Busy 1 = Ready
5	ARDY	ARDY	ARDY	ARDY	ARDY	Don't Care
4	-	-	-	-	-	Don't Care
3	-	-	Rewrite recommended	-	-	0 = Normal or uncorrectable 1 = Rewrite recommended
2	-	-	-	-	-	Don't Care
1	FAILC (N-1)	FAILC (N-1)	Reserved	-	-	Don't Care
0	FAIL	FAIL (N)	FAIL	-	FAIL	0 = Successful PROGRAM / ERASE / READ 1 = Error in PROGRAM / ERASE / READ

Notes:

1. For simplicity, the acronym "SR" is used throughout the document to denote Status Register.
2. SR[6] is 1 when the cache is ready to accept new data.
3. R/B# follows the value of SR[6].
4. SR[5] is 0 during program operation. In cache mode, this bit is 1 when all internal operations are complete.
5. SR[0] being FAIL signifies that an uncorrectable error has occurred.
6. SR[6] and SR[5] are shared by all planes on the die (LUN) selected by Read Status Enhanced 78h command.
7. SR[1] and SR[0] are specific to the plane specified by the row address, which comes with the Read Status Enhanced 78h command.

2.14. Block Lock Feature

The device has block lock feature which protects a specified range of blocks against program and erase operations. It is preferable to using WP# pin for memory protection.
This feature is determined by the status of LOCK pin at power-up. LOCK being Low at power-up will disable all Block Lock commands. LOCK being High at power-up will enable Block Lock commands, and all blocks are protected by default, regardless of the value of WP# pin. Locked blocks can be locked tight, which disables any locking or unlocking operations on the devices blocks.
In order to modify the content of the memory array of the NAND Flash, unlock operation should be performed.

Program and erase operations take effect only in unlocked address space.

2.14.1. WP# and Block Lock

The rules of WP# and Block Lock mechanism is listed as follows.

1. If the blocks are not locked tight, then holding WP# Low locks all blocks.
2. If WP# goes Low and High again, then a new Unlock command is needed to unlock blocks if program or erase operations are desired.

2.14.2. Boundary Block Address Registers And Invert Area Bit

The range of unlocked blocks is defined by two registers and one control bit:

1. Upper boundary block address register;
2. Lower boundary block address register (must be less than the upper boundary block address register);
3. Invert area bit.

If invert area bit is 0, then the address range between the two registers are unlocked. Otherwise if invert area bit is 1, then the address range outside the two registers are unlocked. See the figures below for demonstration for this mechanism.

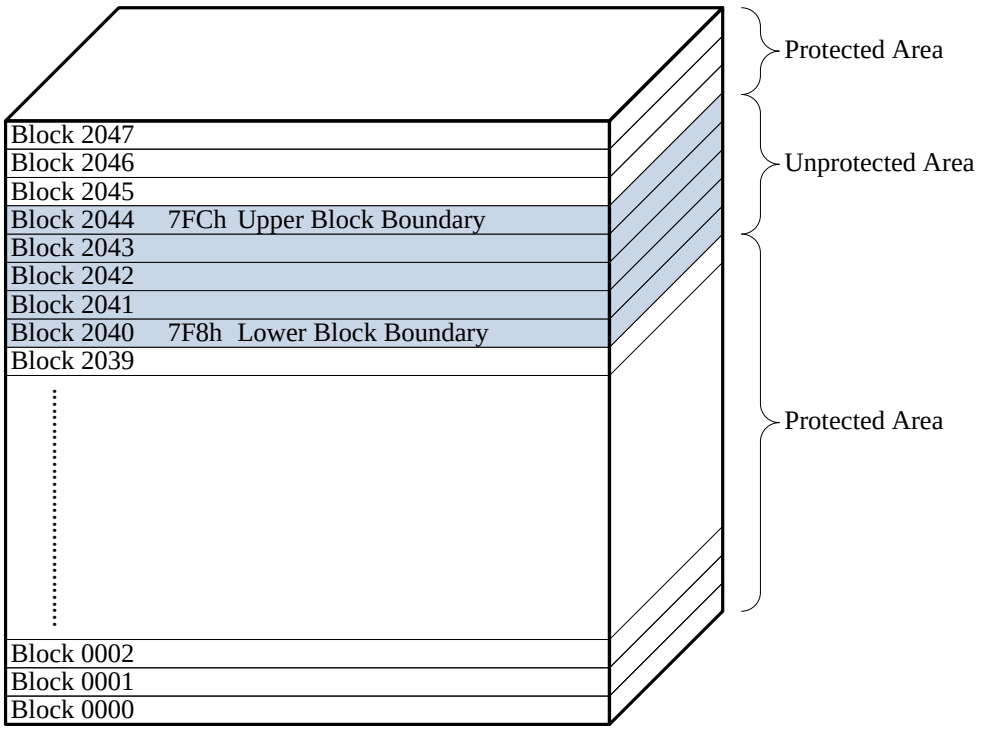

Figure 4: Flash Array Protected: Invert Area Bit = 0

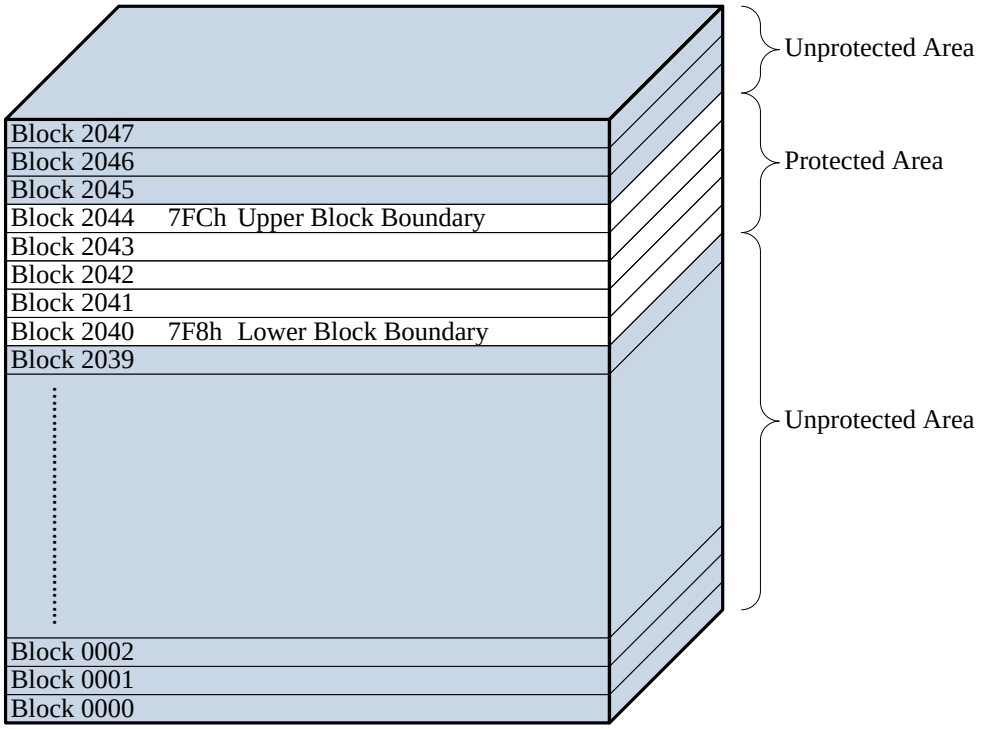

Figure 5: Flash Array Protected: Invert Area Bit = 1

2.14.3. Block Lock Addressing

The address cycles that accesses the boundary block address registers are defined in the following table. Address cycles following Unlock 23h and 24h commands indicate the lower and upper boundary block address registers, respectively. The LSB of page address corresponds to the invert area bit.

The device allows only one range to be specified by the boundary block address registers. After 23h and 24h unlock commands has taken effect, if more 23h or 24h commands are issued, then these registers will be updated with new values.

Table 16: Block Lock Addressing

Bus Cycle	IO[7]	IO[6]	IO[5]	IO[4]	IO[3]	IO[2]	IO[1]	IO[0]
1st Cycle	BA[7]	BA[6]	Low	Low	Low	Low	Low	Invert Area Bit
2nd Cycle	BA[15]	BA[14]	BA[13]	BA[12]	BA[11]	BA[10]	BA[9]	BA[8]
3rd Cycle	Low	Low	Low	Low	Low	Low	BA[17]	BA[16]

Notes:

1. The Invert Area Bit is valid in 24h command. It may be Low or High in 23h command.

2.14.4. Block Lock Status Register

Block lock status register contains detailed information of the lock or unlock status of a block. The host can poll this register to learn the protection status of a specific block.

Table 17: Block Lock Status Register Bit Definition

Block Lock Status Register Definition	IO[7:3]	IO[2] (Lock#)	IO[1] (LT#)	IO[0] (LT)
Block is locked tight	X	0	0	1
Block is locked	X	0	1	0
Block is unlocked, and device is locked tight	X	1	0	1
Block is unlocked, and device is not locked tight	X	1	1	0

Notes:

1. LT is acronym for Lock Tight.

2.14.5. Block Lock Flow

The control flow of block lock mechanism is summarized in the following figure.

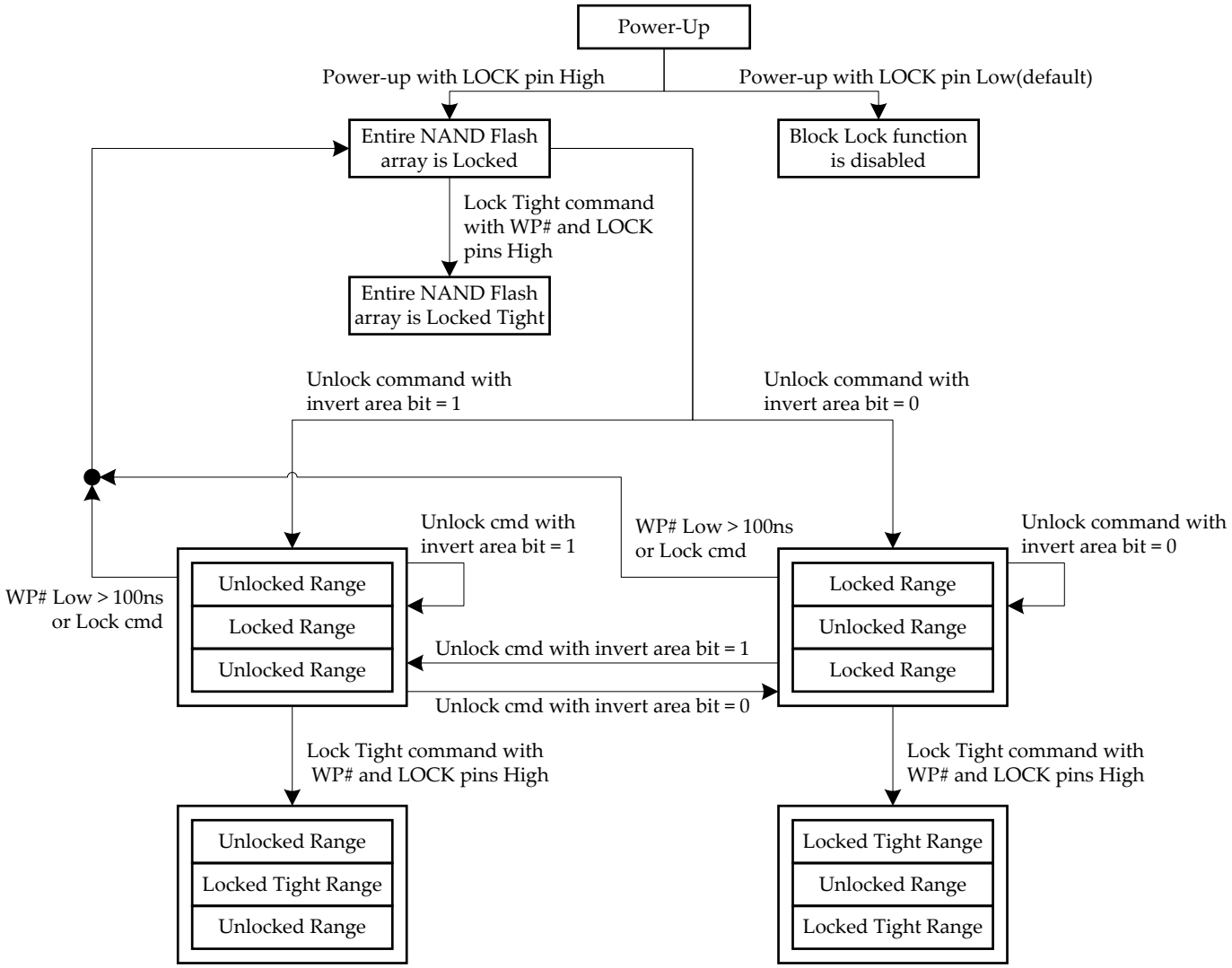

Figure 6: Block Lock Flowchart

3. Bus Operations

3.1. Asynchronous Interface Mode Selection

The mode selection of the bus interface is summarized in the following table.

Table 18: Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	IOx	WP#
Standby	H	X	X	X	X	X	0V/Vcc
Command Input	L	H	L	⎍	H	X	H
Address Input	L	L	H	⎍	H	X	H
Data Input	L	L	L	⎍	H	X	H
Data Output	L	L	L	H	⎎	X	X
Write Protect	X	X	X	X	X	X	L

Notes:

1. H = Logic level HIGH; L = Logic level LOW; X = Logic level HIGH or LOW.

2. WP# should be biased to CMOS Low or High for standby.

The mode selection table is graphically interpreted in the following figures in order to aid understanding. Detailed timing diagrams for the various bus modes will be presented in later section.

3.2. Standby

It is a typical practice to drive CE# pin to HIGH when the device is not performing an operation, which puts the devices in standby mode. In standby mode the device is deselected, outputs are disabled, and the device operates at reduced power consumption.

The device has CE# "Don't Care" capability that allows the NAND Flash to share the asynchronous bus with other memory devices: While the current NAND Flash is busy in its internal operations, other devices on the same bus can be accessed. This feature enables the designer to place multiple NAND Flash devices on one asynchronous bus.

3.3. Asynchronous Command Input

Asynchronous command input cycle issues a command to the device, instructing it to perform a certain action. Commands are loaded from IO[7:0] to internal command register by WE# rising edge when CE# is low, CLE is high, ALE is low and RE# is high.

While the device is busy (RDY=0), only Read Status and Read Status Enhanced commands are accepted, while other commands are typically ignored. For commands that modifies (write or erase) any contents in the memory, WP# pin must be high.

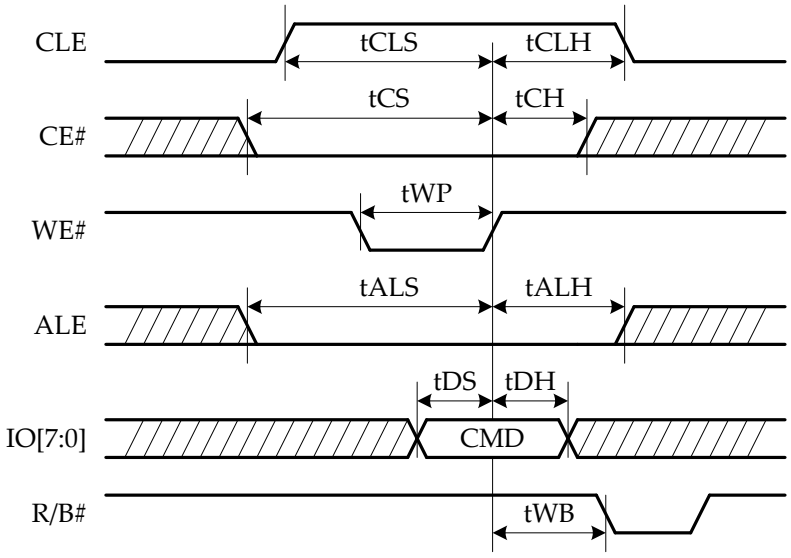

Figure 7: Asynchronous Command Input Cycle Timing Diagram

3.4. Asynchronous Address Input

Asynchronous address input cycle allows the host to feed the address of a read, program or erase operation to the device. Addresses are loaded from IO[7:0] to internal address register on the rising edge of WE# when CE# is low, ALE is high, CLE is low and RE# is high.

Bits that do not belong to valid address space must be set to low. The number of address cycles is dependent on the command it belongs to; refer to command descriptions for detailed requirements of address cycles.

While the device is busy (RDY=0), only the address of Read Status Enhanced command is accepted, while the address cycles of other commands are typically ignored.

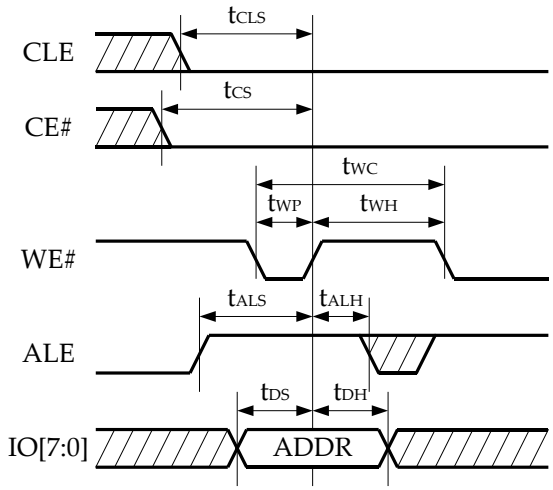

Figure 8: Asynchronous Address Input Cycle Timing Diagram

3.5. Asynchronous Data Input

The asynchronous bus feeds data to the device on WE# rising edge when CE# is low, ALE is low, CLE is low and RE# is high. Input data may be used to program the device memory array, or to modify device configurations. If Program operation is to be performed, WP# pin should be high during data input cycles.
While the device is busy (RDY=0), data input is ignored by the device.

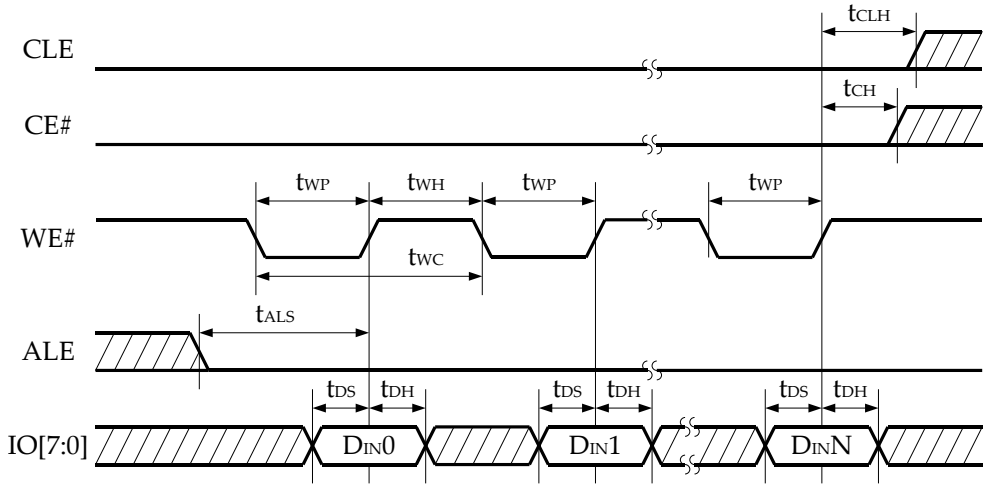

Figure 9: Asynchronous Data Input Cycle Timing Diagram

3.6. Asynchronous Data Output (Normal)

Data output operation transfers data, Status register, among other configuration information, from the device to the host. Data bytes can be shifted out of the device in a serial manner on RE# falling edge when CE# is low, ALE is low, CLE is low, and WE# is high.
If the host drives RE# high so that t_{RC} >= 30ns, then the host can latch the data on RE# rising edge, see the timing diagram below, which illustrates normal output mode.

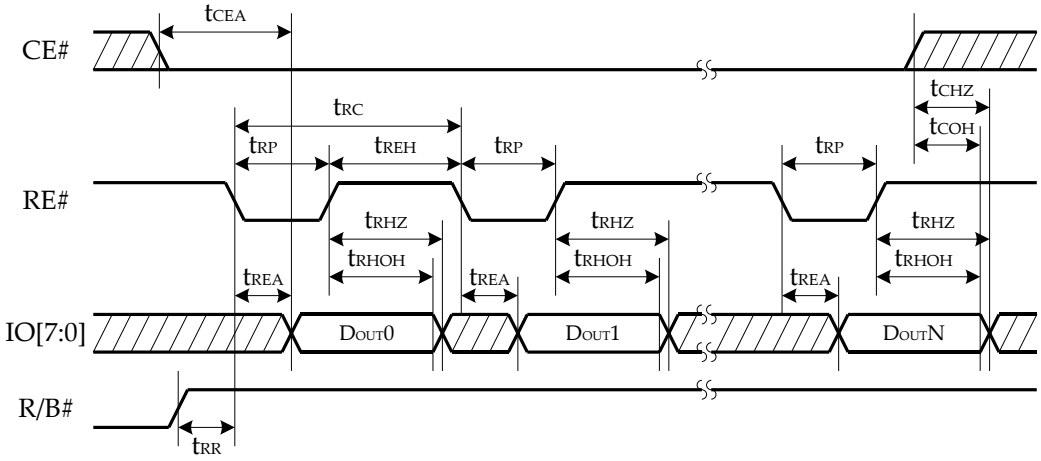

Figure 10: Asynchronous Data Output Cycle (Normal) Timing Diagram

3.7. Asynchronous Data Output (EDO)

During read operations, if RE# is driven in such a way that t_{RC} < 30ns, then the host can latch data on the next falling edge of RE# (Extended Data Output, EDO mode).

It should be noted that the device gives no indication whether it is in normal or EDO mode, nor does it indicate when output data is valid or when it is not. It is up to the host designer to sample output data at correct time.

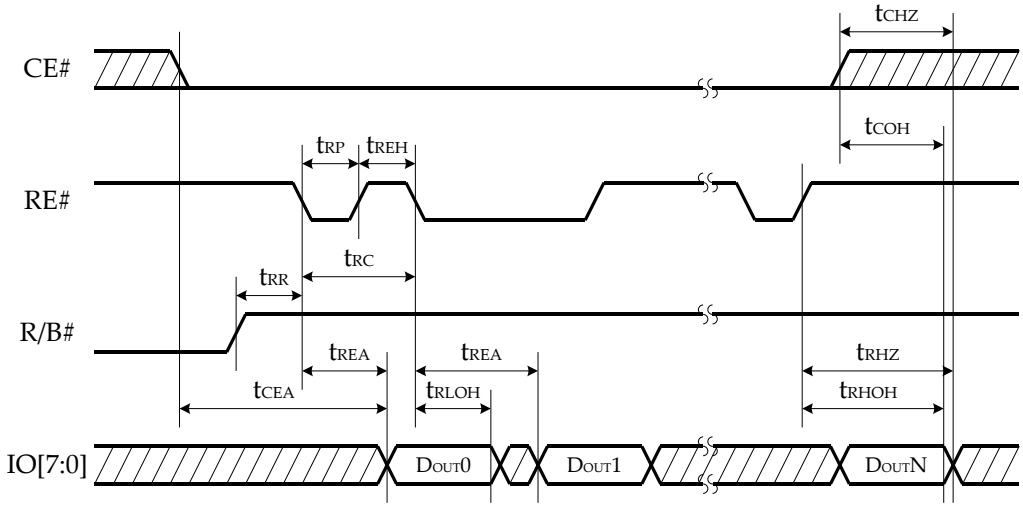

Figure 11: Asynchronous Data Output Cycle (EDO) Timing Diagram

3.8. Write Protect

Hardware Write Protection is enabled when WP# is low. While the device is protected, all Program and Erase commands are ignored and the content of the memory array is protected against any modification. It is recommended to drive WP# low during power-up to protect the device against inadvertent Program and Erase operations.

If WP# is low or toggled low during Read operations, read is not interrupted and will behave as normal.

If WP# is toggled during Program or Erase operations (R/B# is low):

1. The Program or Erase operation is aborted.
2. The data being programmed or erased becomes invalid.
3. The SR becomes 60h until a Reset command, a new operation or power-cycling is applied to the device.
4. In asynchronous mode, toggling WP# low during Program or Erase operations is equivalent to a Reset (FFh) command; in synchronous mode, it is equivalent to Synchronous Reset (FCh) command.

3.9. Ready/Busy#

The ready/busy# (R/B#) pin indicates whether a target is ready or busy. When R/B# is Low, the target is "busy" (RDY=0), which is defined as one or more of LUNs being busy with internal operations; when R/B# is High, the target is "ready", which is defined as all LUNs being ready (RDY=1). Besides, the status of each LUN can also be determined by polling the Status Register of the corresponding LUN.

R/B# is an open-drain signal that allows the R/B# pins of multiple devices to be tied together and create wired-OR logic. R/B# requires an external pull-up resistor to pull it high when the device releases the pin to high impedance state. The rise time of R/B# when it is pulled high is determined by RC constant T_C:

$$T_C = R_P \times C$$

Where R_P is the resistance of the pull-up resistor, and C is the capacitive loading of R/B#.

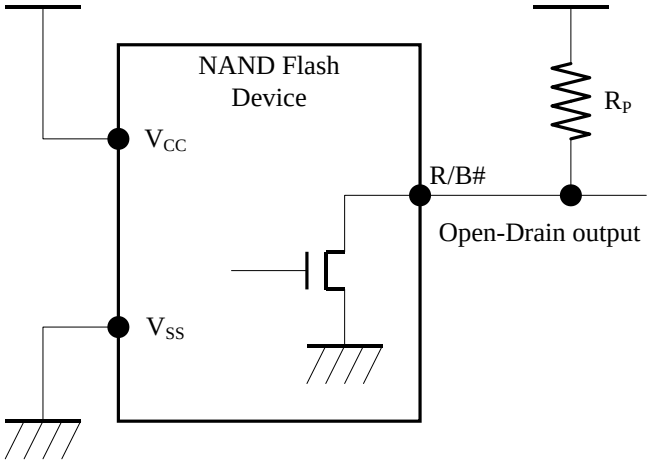

Figure 12: R/B# Open-Drain Output

The value of R_P can be calculated using the following equation:

$$R_P = \frac{V_{CC}(MAX) - V_{OL}(MAX)}{I_{OL} + \sum I_L}$$

Where $\sum I_L$ is the sum of all input currents to the R/B# pin.

4. Device Operations

4.1. Reset

4.1.1. Reset (FFh)

Writing FFh command performs Reset operation on the device, which aborts all operations in progress and puts the device into a known status.

After Reset command, the command register is cleared and is available to accept the next incoming command. If Reset command is sent while the device is in Program or Erase operations, then the contents of the targeted flash memory location may be invalid due to partially terminated operations.

Following FFh command, the device drives R/B# low for t_{RST}. After device power-up, the Reset command must be the first command issued to all CE#s, after which the device will be in busy state for 1ms max.

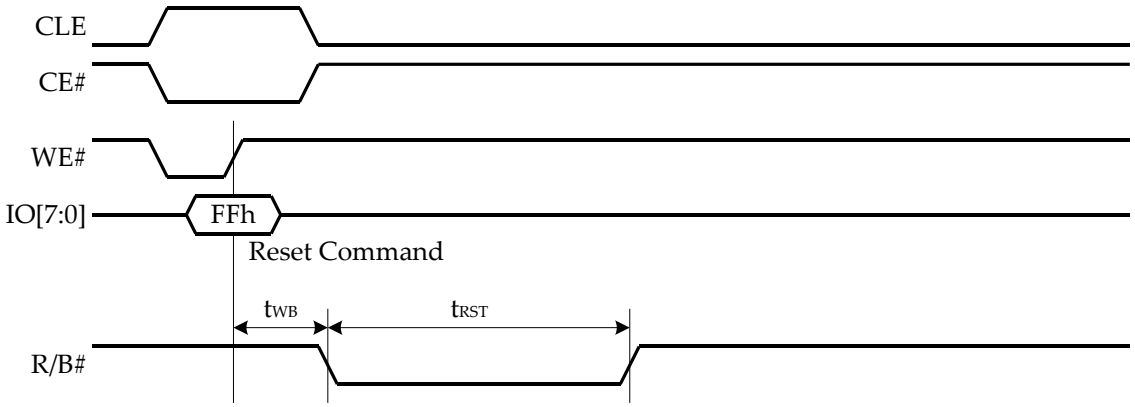

Figure 13: Reset (FFh) Timing Diagram

4.2. Read ID (90h)

The Read ID 90h command reads ID information which is preprogrammed into the device. The command is accepted only when all LUNs of the target are idle.

A combination of 90h command and 00h address outputs 5-byte ID code that includes device Manufacturer ID, device configuration, and part-specific information.

A combination of 90h command and 20h address outputs 4-byte ID code that corresponds to ONFI Signature.

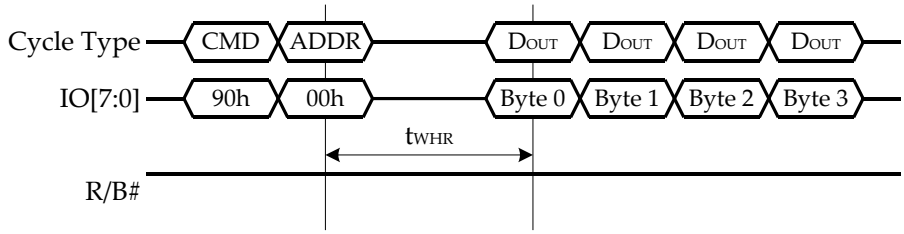

Figure 14: Read ID Operation: Manufacture ID

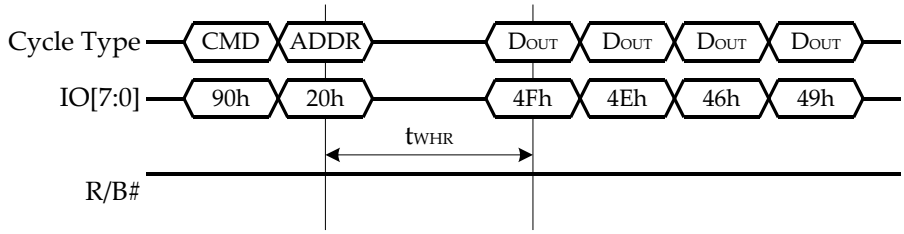

Figure 15: Read ID Operation: ONFI Signature

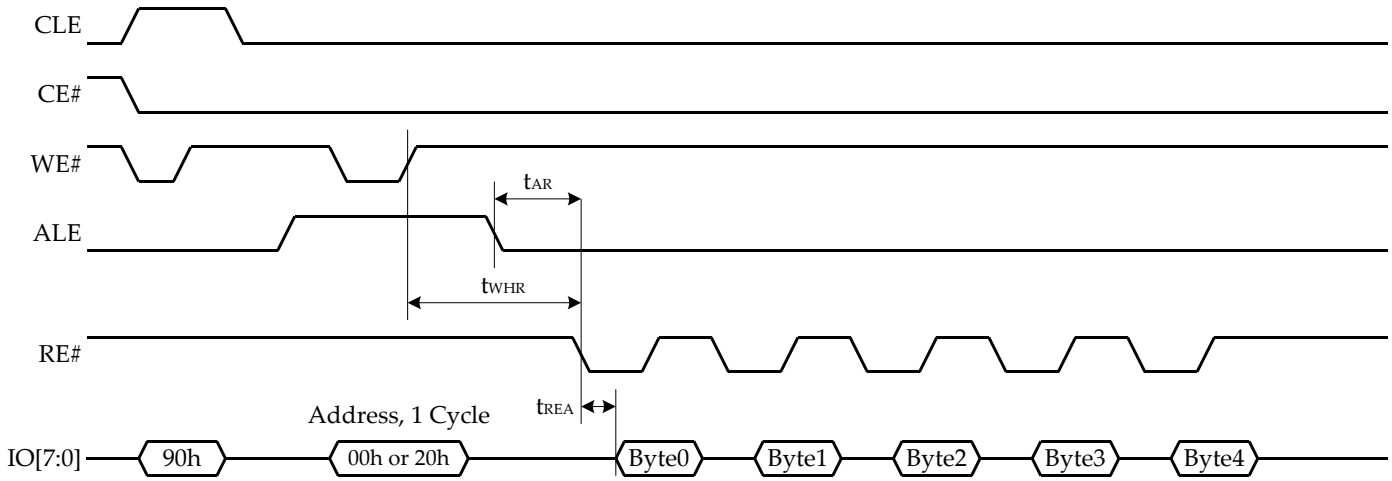

Figure 16: Read ID Timing Diagram

4.3. Read Parameter Page (ECh)

The Read Parameter Page ECh command reads the ONFI parameter page preprogrammed into the device. The command is acceptable only when all LUNs of the target are idle.

Writing ECh command and 00h address puts the device in Read Parameter Page mode, with R/B# pulsed low for a duration of t_R, which indicates that the device is busy retrieving the internal data structure. After R/B# goes high again, parameter page information is ready to be shifted out of the device on consecutive RE# falling edges. The target stays in the Read Parameter Page mode until another valid command is input to the device.

While the device is busy during t_R, the Read Status (70h) command can be used to poll the device and check the status for command completion, after which the Read Mode (00h) command must be issued to place the device back into data output mode. However, the Read Status Enhanced (78h) command should not be used during the execution of ECh command.

To guarantee data storage reliability, the device has many copies of the parameter page. If the device returns incorrect parameter page data in response to an initial ECh command, the command can be reissued to read the next parameter page. The process can be repeated until a correct copy is retrieved.

During read operations, the Random Data Read (05h-E0h) command can be issued to move to a different column address for data output.

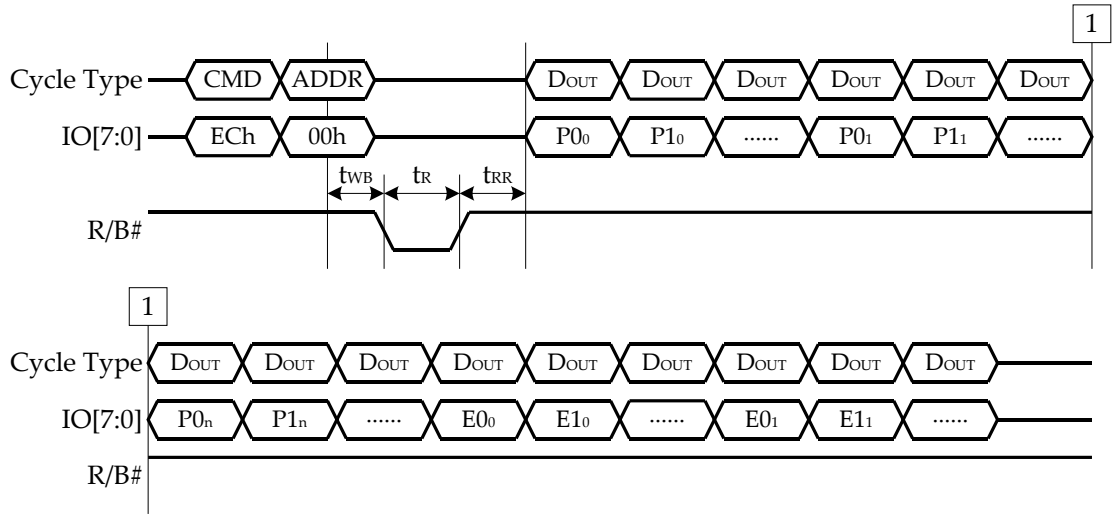

Figure 17: Read Parameter Page Operation

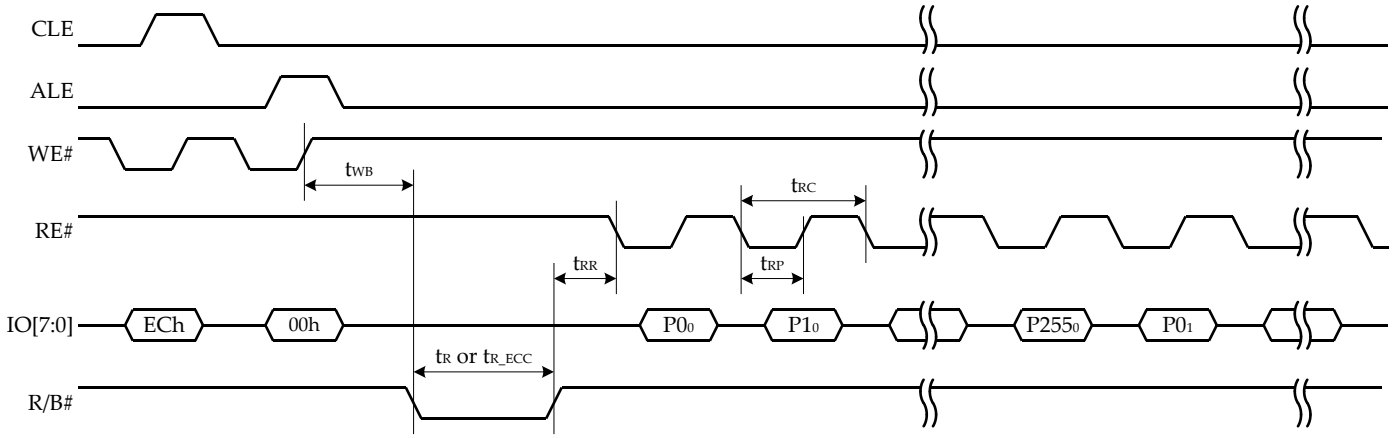

Figure 18 Read Parameter Page Timing Diagram

4.4. Read Unique ID (EDh)

The Read Unique ID (EDh) command retries a series of 16 byte Unique IDs from the device. The command is

acceptable only when all LUNs of the target are idle.

Writing ECh command and 00h address places the device into busy state with R/B# being low for a duration of t_R. After R/B# goes high again, data is shifted out of the device for every RE# toggle.

While the device is busy, the Read Status (70h) command can be used to check the device for command completion status. After 70h is finished, Read Mode (00h) command should be issued to allow the device to continue with data output.

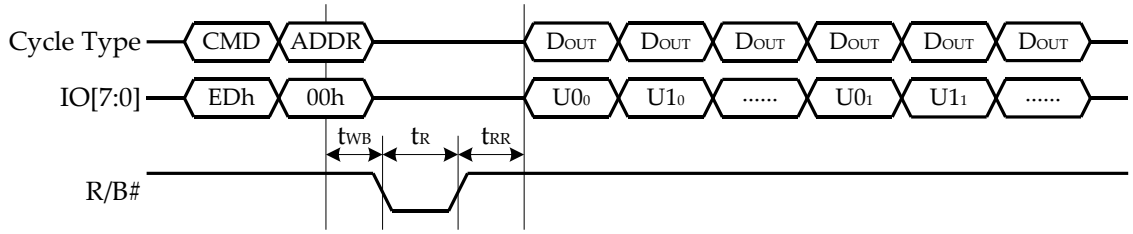

Figure 19: Read Unique ID Operation

4.5. Feature Operations

Get feature and set feature commands enables the host to access the feature table in the device.

4.5.1. Get Features (EEh)

Command EEh combined with a feature address byte reads the specified subfeature parameters (P1 through P4) from the address. The device goes busy for a minimum of t_{FEAT}, after which feature data bytes are ready to be retrieved from the device. The Read Status (70h) command can be used to monitor the device for command completion; after 70h command is complete a Read Mode (00h) command should be issued to place the device back into data output mode.

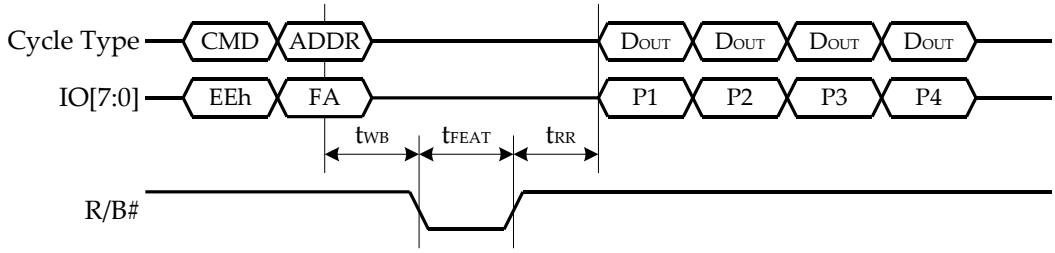

Figure 20: Get Feature Operation

4.5.2. Set Features (EFh)

Writing EFh command in combination with one of the feature addresses puts the device in Set Features mode; after a minimum delay of t_{ADL}, subfeature parameters P1 through P4 can be input to the device. After all parameter data are input, the target becomes busy for t_{FEAT}. The Read Status (70h) command can be issued to poll the device for command completion status.

Subfeature parameter information is volatile; by default, the feature value written to the device remains valid until the device is power cycled. Once set, the feature value remains valid even if a Reset (FFh) command is issued, unless the feature table specifies otherwise.

The EFh command and address 90h can be used to enable or disable the internal ECC of the device.

Among available feature addresses, 01h (timing mode) is unique: If EFh is used to modify the interface type, the target will be busy for t_{ITC}.

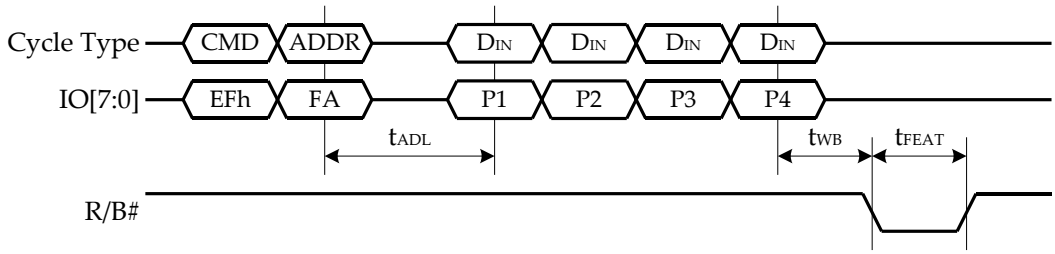

Figure 21: Set Features Operation

4.6. Status Operations

4.6.1.Read Status (70h)

Each die (LUN) of the device has its own 8-bit status register. The Read Status 70h command accesses the status value of the last-selected die (LUN) of the target. If the current target has only one die (LUN), then 70h can be used to retrieve the device status after any NAND command. The command is accepted by the addressed die (LUN), and can be issued even when the device is busy (RDY=0).

The 70h command outputs the contents of the Status Register of the most recently selected LUN. During interleaved die (multi-LUN) operations, only one die (LUN) can be enabled for SR output to prevent data contention. To select a specific die for SR output, Read Status Enhanced (78h) command can be used.

When 70h command is used to check the status of a read operation during execution, the device remains in SR output mode until another valid command is received; in such case, a read mode command 00h should be issued to bring the device back to read operation and continue with the data output flow.

When internal ECC is enabled, 70h command is required after t_{R_ECC} of data transfer to detect whether an uncorrectable read error is encountered.

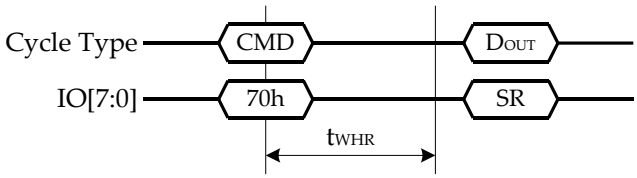

Figure 22: Read Status Operation

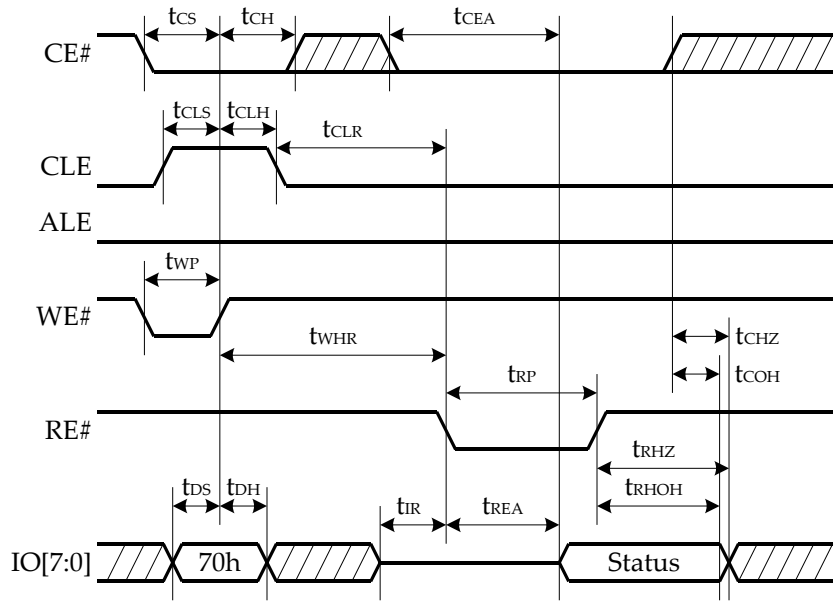

Figure 23: Read Status Timing Diagram

4.6.2.Read Status Enhanced (78h)

The Read Status Enhanced 78h command is used with three row address cycles including page, block and LUN addresses to select the specified die (LUN) and put it in read status mode; unselected dies (LUNs) are disabled to avoid bus contention. The addressed die remains in this mode until another valid command is accepted.

For a multi-LUN device, the 78h command outputs the contents of the Status Register of the addressed LUN, and the host may also use this command for LUN selection. This command is accepted by all dies (LUNs), even when the device is busy (RDY=0).

The 78h command also enables the addressed die (LUN) for data output. During a Read-series operation, after the addressed die (LUN) is ready (RDY=1), issuing Read Mode 00h command places the device back in data output mode.

The 78h command is prohibited in the following situations:

1. During power-on Reset FFh command.
2. When OTP mode is enabled.
3. After some other reset, ID and configuration commands; see command descriptions for detail.

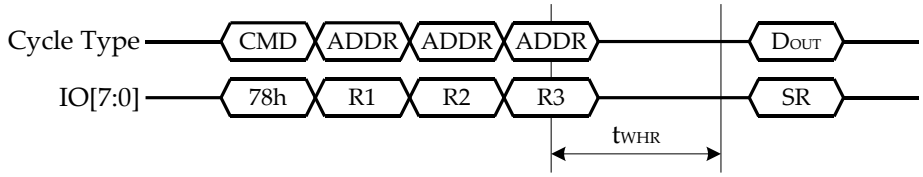

Figure 24: Read Status Enhanced Operation

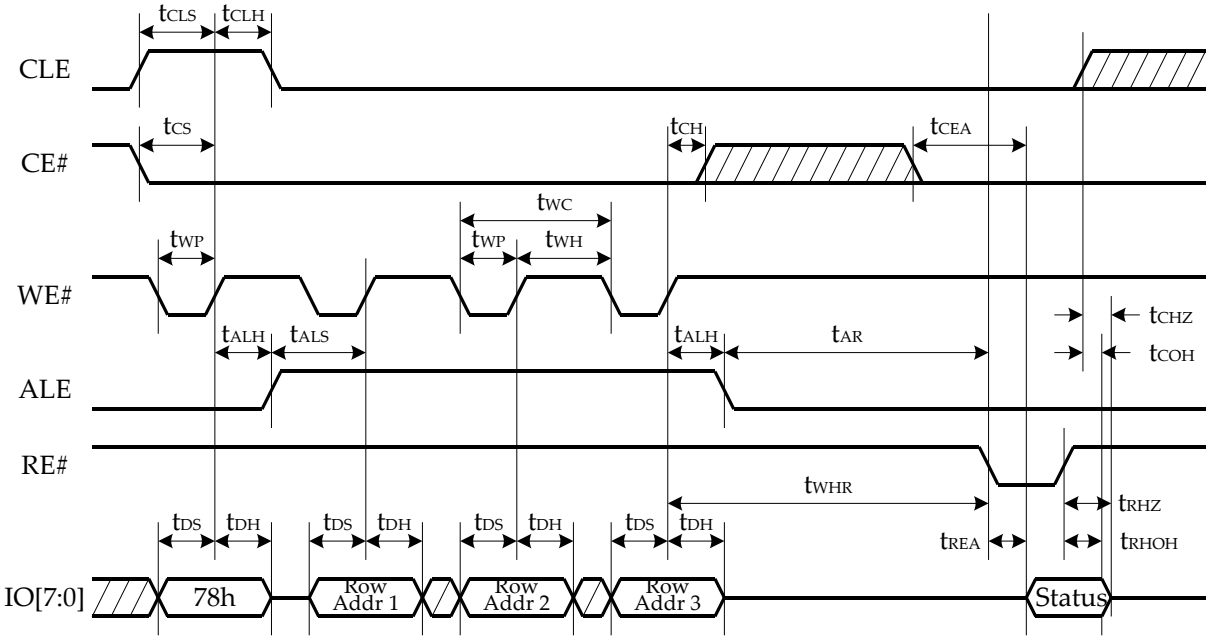

Figure 25: Read Status Enhanced Timing Diagram

4.7. Column Address Operations

The column address operations allows access to the data from the cache register in the select die (LUN), which enables the host greater flexibility in data manipulation, and allows the host to take advantage of the NAND Flash internal cache register if the host buffer is small.

With asynchronous interface active, any byte in the selected cache register can be accessed via column address operations.

4.7.1.Random Data Read (05h-E0h)

While data is shifted out of the cache register, the host can change the column address to be output by issuing 05h-E0h commands. The two column address cycles specify the column address to read. This command is accepted by the selected die (LUN) when it is ready (RDY=1, ARDY=1), or during Cache Read oeprations (Rdy=1, ARDY=0).

After E0h command, the host should wait for at least t_{WHR} before driving output data. The selected die (LUN) remains in data output mode until another valid command is received.

If the target has more than one die (LUN), then for interleaved die (multi-LUN) operations the Read Status Enhanced (78h) command should be issued prior to 05h-E0h to avoid bus contention.

The behavior of Random Data Read command is shown below.

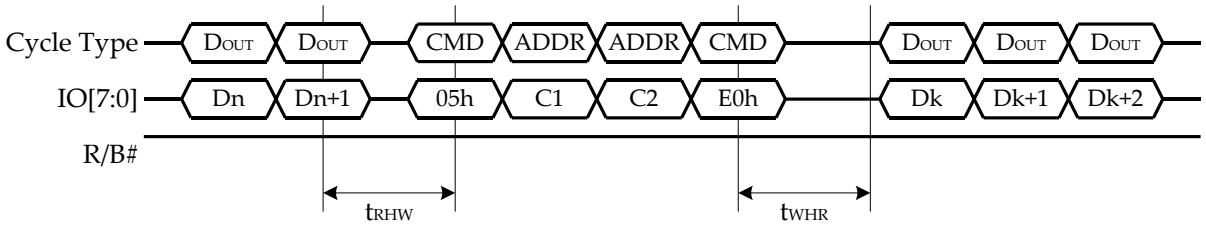

Figure 26: Random Data Read Operation

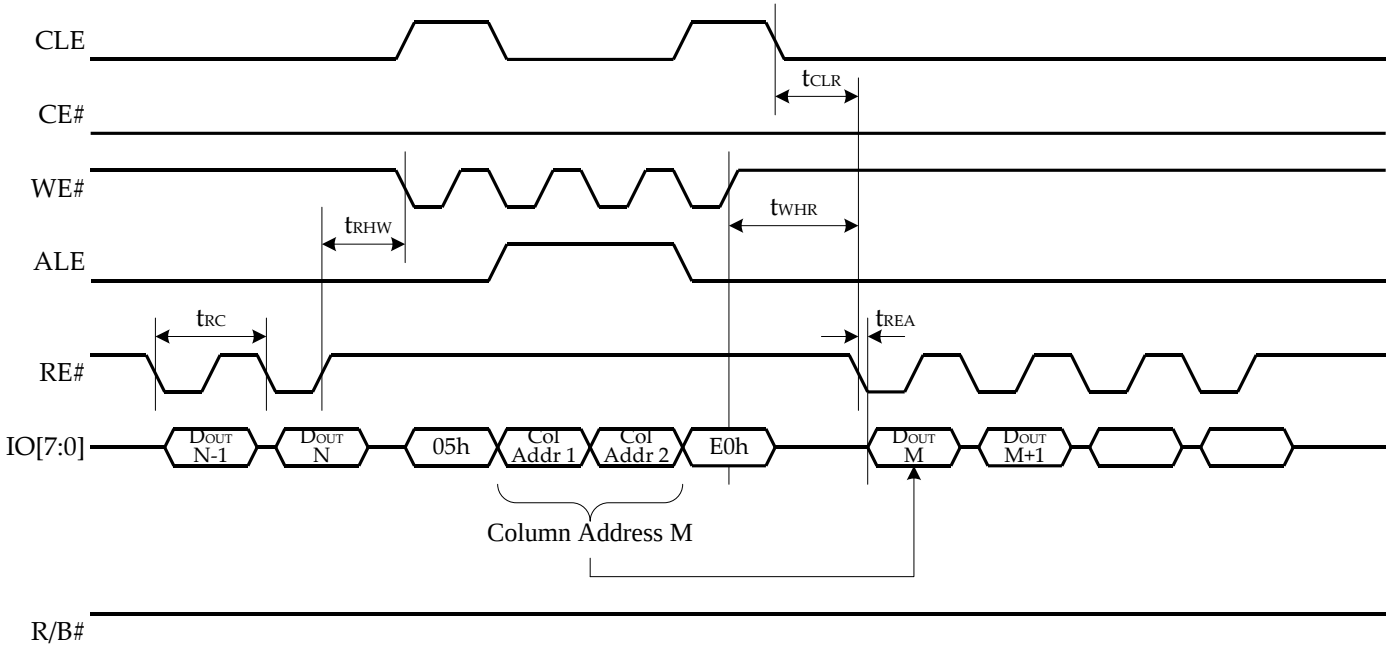

Figure 27 Random Data Read Timing Diagram

4.7.2.Random Data Read Two-Plane (06h-E0h)

The Random Data Read Two-Plane command 06h-E0h changes the LUN, plane and column addresses of a Read command operation. Two column and three row address cycles enables data output at the specified column address. This command is accepted by a die (LUN) when it is ready (RDY=1, ARDY=1).

After E0h command, the host should wait for at least t_{WHR} before driving output data. The selected die (LUN) remains in data output mode until another valid command is received.

If the target has more than one die (LUN), the 06h-E0h command can be used after an interleaved die (multi-LUN) read operation when all dies (LUNs) are ready (RDY=1). Dies (LUNs) not accessed are deselected to avoid bus contention.

If the target has more than one die (LUN), then for interleaved die (multi-LUN) operations with more than one

dies (LUNs) being busy (RDY=1, ARDY=0 or RDY=0, ARDY=0), the Read Status Enhanced 78h command should be issued to select a certain die (LUN) before the 06h-E0h command, otherwise bus contention may occur.
This command is not applicable for single-LUN devices.

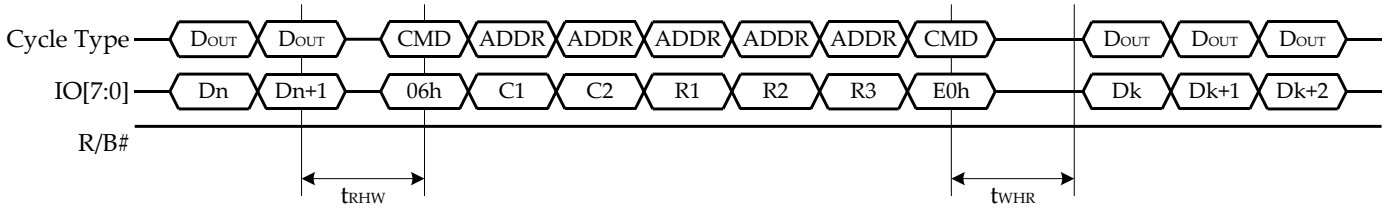

Figure 28: Random Data Read Two-Plane Operation

4.7.3.Random Data Input (85h)

During data input cycles, the host can change the destination column address by issuing the 85h command followed by two address bytes, which is interpreted as the column address for upcoming data stream. This command is accepted by a die (LUN) when it is ready (RDY=1, ARDY=1), or during cache program operations (RDY=1, ARDY=0).
After the last byte of the new address is input, the host must wait for at least t_{ADL} before feeding input data bytes. The selected die (LUN) remains in data input mode until another valid command is received.
For Program Page (80h-10h), Program Page Cache (80h-15h), Program For Internal Data Move (85h-10h) and Program For Two-Plane Internal Data Move (85h-11h) commands, the Random Data Input 85h command is acceptable during data input cycles.

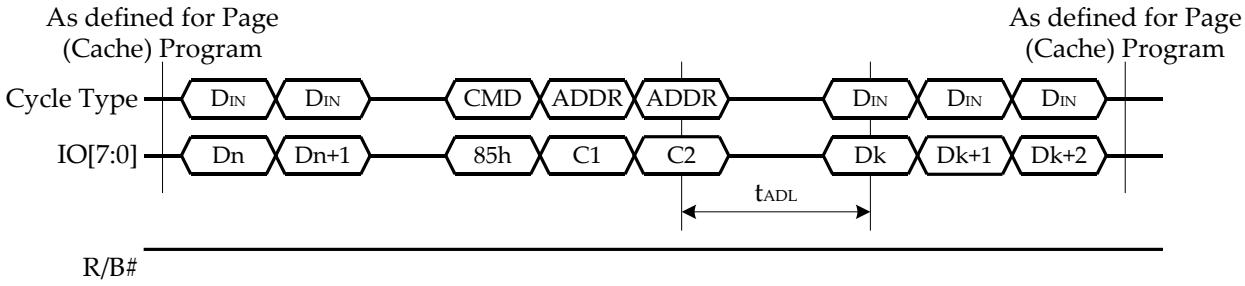

Figure 29: Random Data Input Operation

4.7.4.Program For Internal Data Input (85h)

The Program For Internal Data Input command 85h changes both row and column address during the current program command sequence, and enables data input on the specified die (LUN). This command is accepted by a die (LUN) when it is ready (RDY=1, ARDY=1), or during cache program operations (RDY=1, ARDY=0).
After the last byte of the new address is input, the host must wait for at least t_{ADL} before feeding input data bytes. The selected die (LUN) remains in data input mode until another valid command is received.
For Program Page (80h-10h), Program Page Two-Plane (80h-11h), Program Page Cache (80h-15h), Program For Internal Data Move (85h-10h) and Program For Two-Plane Internal Data Move (85h-11h) commands, the 85h command is acceptable between these commands' address cycles and the final command cycle (10h, 11h, 15h).
The 85h command allows the host to change the original address of the data in the cache register and reroute it to a new address.
If the target has more than one die (LUN), the 85h command should be used with commands that support interleaved die (multi-LUN) operations.
When used in conjunction with Random Data Read 05h-E0h or Random Data Read Two-Plane 06h-E0h commands, the 85h command allows the host to read and modify the cache register contents prior to program

operations, reducing the buffer size required in the host controller.

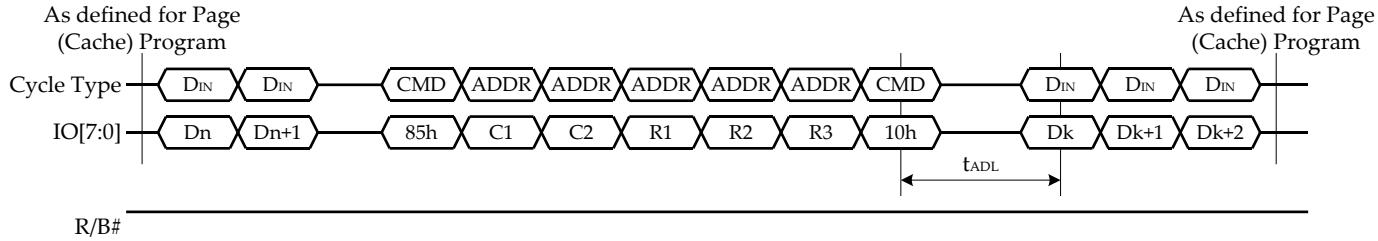

Figure 30: Program for Internal Data Input Operation

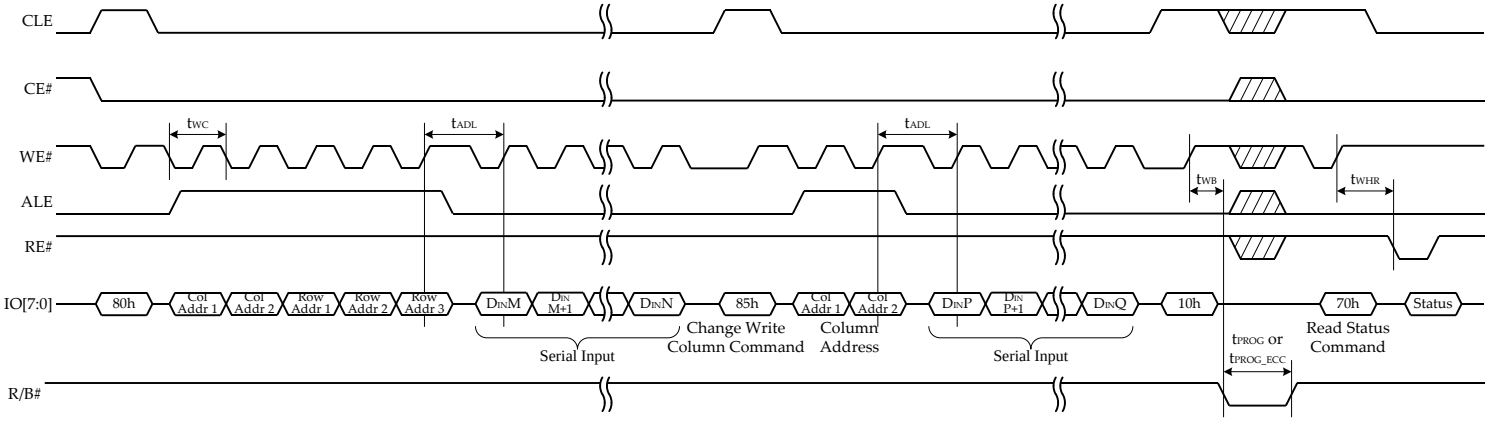

Figure 31: Program Page with Random Data Input Timing Diiagram

4.8. Read Operations

The host uses read commands to acquire data stored in the flash memory array. The Read Page (00h-30h) command reads one page from the device to the cache register, and allows data in cache register to be output. While data is output, Random Data Read (05h-E0h) and Random Data Input (85h) commands can be issued to read and modify the data in cache registers.

Read operations fall into several categories, which will be explained in further detail in the following sections.

4.8.1.Read Mode (00h)

If a Read operation (00h-30h, 00h-3Ah, 00h-35h) is polled with status register by 70h or 78h commands, then the Read Mode (00h) command can be issued to disable the status output and enable the device to output data from the last-select die (LUN). This command is accepted by the die (LUN) when it is ready (RDY=1, ARDY=1) or during Read Page Cache (31h, 00h-31h) commands (RDY=1 and ARDY=0).

While doing interleaved die (multi-LUN) operations for a target with more than one dies (LUNs), the Read Mode (00h) command should be preceded by Read Status Enhanced (78h) command which selects only one die (LUN) and thus prevents bus contention.

4.8.2.Read Page (00h-30h)

The Read Page (00h-30h) command launches a read operation: it first copies a page from the array to the cache register, and then enables data output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY=1, ARDY=1).

The 00h and 30h commands are issued with address cycles between them. After the command sequence, R/B# of the selected die (LUN) is pulsed low for t_R while the device is busy with internal operations. When R/B# is pulsed high again, the host may output cache data by toggling RE# repetitively. The Random Data Read (05h-E0h) command can be issued to modify the read address during data output.

Alternatively, the host may also poll the status register (70h, 78h) to determine when the device is ready to output data. When status register indicates the device is ready (RDY=1, ARDY=1), a Read Mode (00h) command should be issued to disable status output and place the device back in data output mode.

If internal ECC is enabled, the Read Status (70h) command should be used after t_{R_ECC} data transfer to detect whether an uncorrectable read error is encountered.

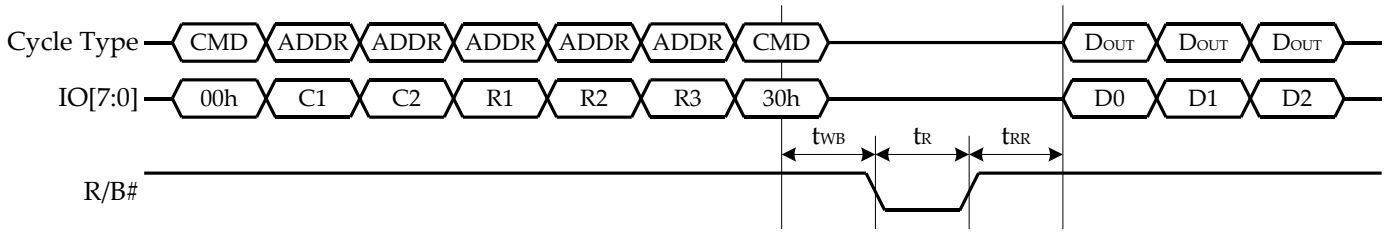

Figure 32: Read Page Operation

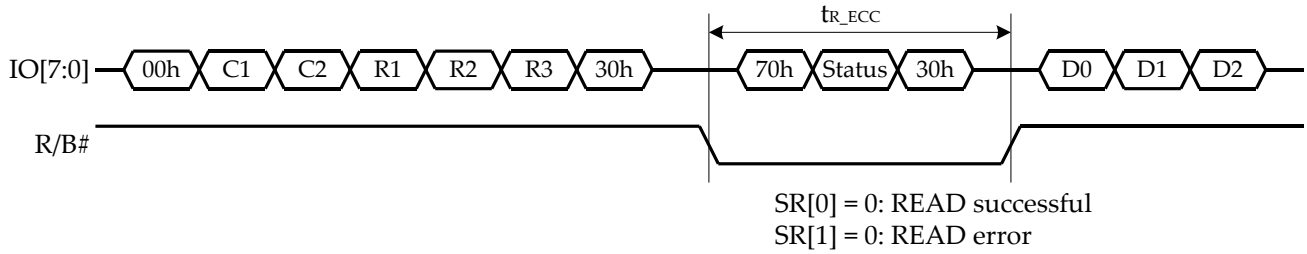

Figure 33: Read Page (00h-30h) Operation with Internal ECC Enabled

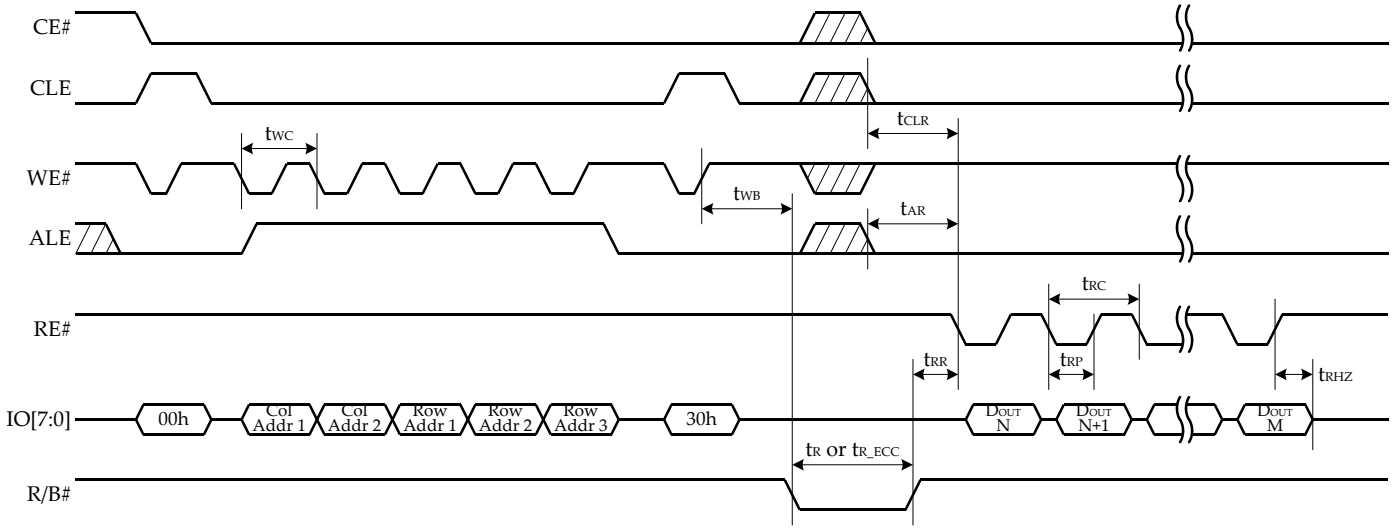

Figure 34 Read Page Timing Diagram

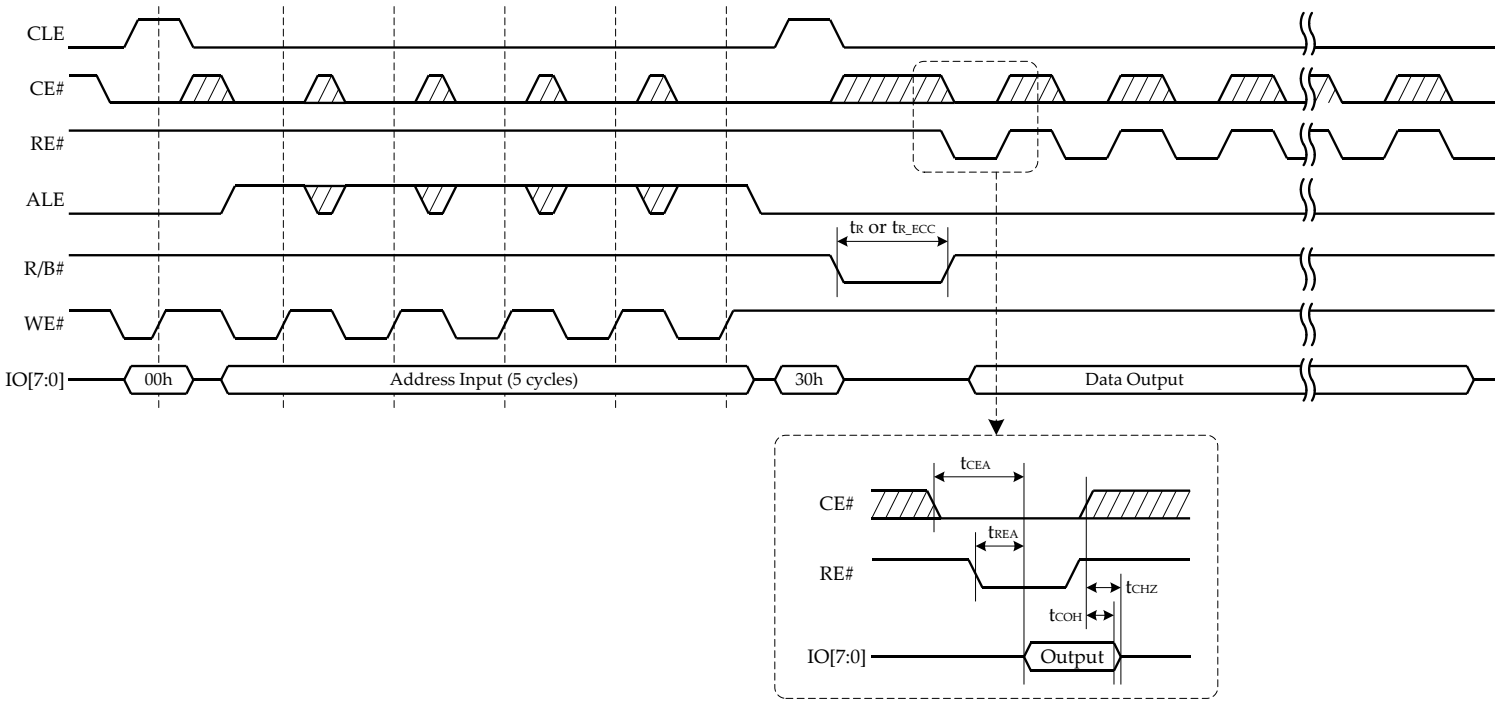

Figure 35 Read Page With CE# "Don't Care" Timing Diagram

4.8.3.Read Page Cache Sequential (31h)

The Read Page Cache Sequential (31h) command allows the next sequential page within a block to be read into the data register, while the previous page is being output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY=1, ARDY=1) or during Read Page Cache (31h, 00h-31h) operations (RDY=1, ARDY=0).

After the 31h command is issued, R/B# goes low for t_{RCBSY} and the die (LUN) is busy (RDY=0, ARDY=0). After R/B# goes high, the status of the die (LUN) becomes busy with cache operation (RDY=1, ARDY=0), which indicates the cache register is available for data output, and the next page is being copied from the memory array to the data register. The Random Data Read (05h-E0h) command can be used to change the read address from the cache register.

The 31h command can read across block boundaries, but not across die (LUN) boundaries. When approaching die (LUN) boundaries, the Read Page Cache Last (3Fh) command should be used.

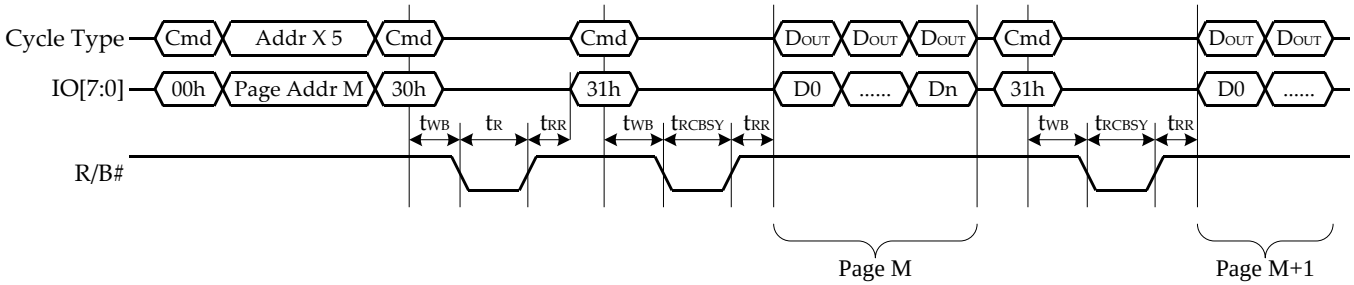

Figure 36: Read Page Cache Sequential Operation

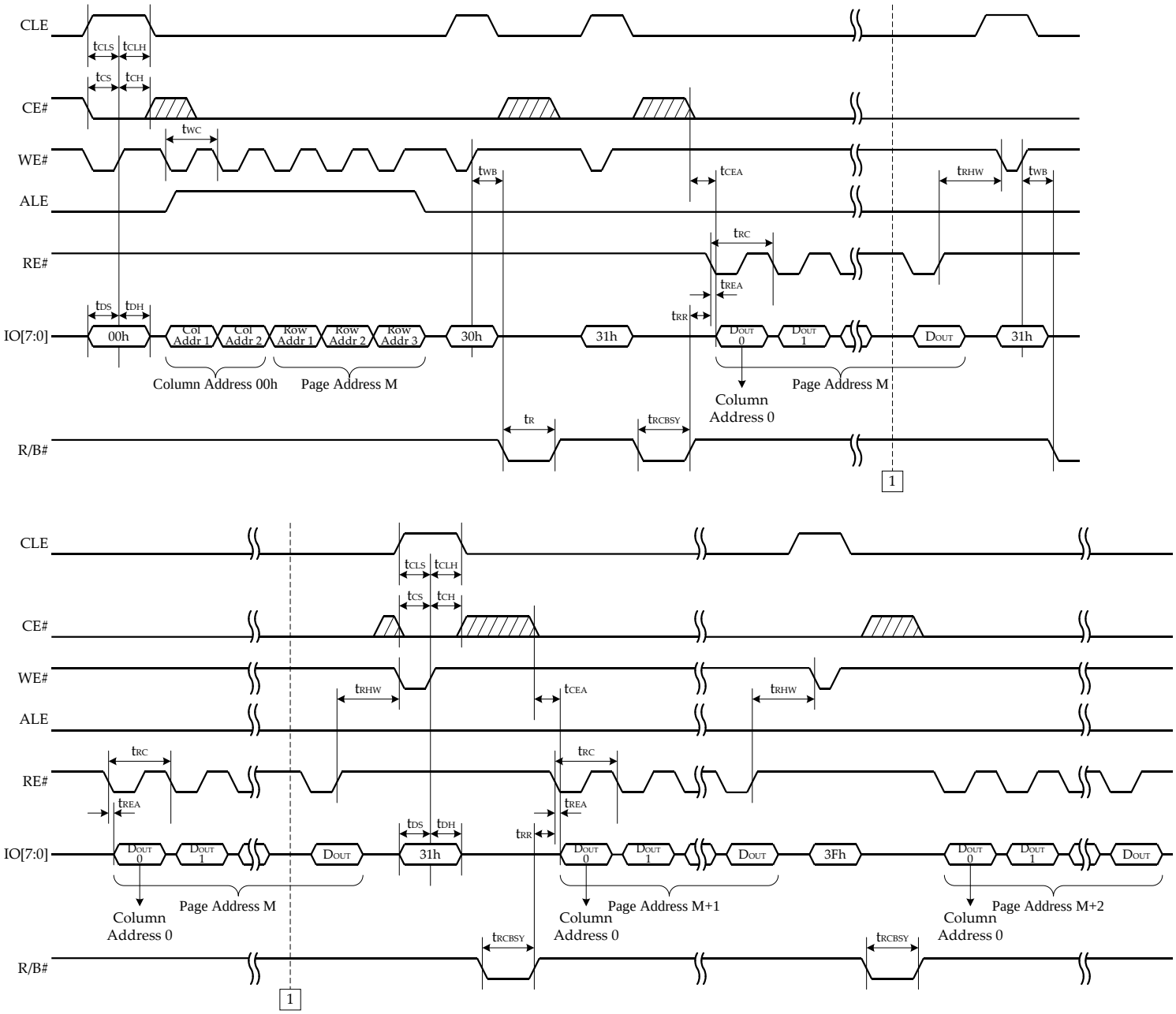

Figure 37 Read Page Cache Sequential Timing Diagram

4.8.4.Read Page Cache Random (00h-31h)

The Read Page Cache Random (00h-31h) command allows the specified page within a block to be read into the data register, while the previous page is being output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY=1, ARDY=1) or during Read Page Cache (31h, 00h-31h) operations (RDY=1, ARDY=0).

The 00h-30h command comes with five address cycles, but the column address is ignored because the command only accesses a page address. This command cannot read across die (LUN) boundaries, so a series of 00h-30h, 00h-31h commands must access the same die (LUN) address.

After the 00h-30h command is issued, R/B# goes low for t_{RCBSY} and the die (LUN) is busy (RDY=0, ARDY=0). After R/B# goes high, the status of the die (LUN) becomes busy with cache operation (RDY=1, ARDY=0), which indicates the cache register is available for data output, and the next page is being copied from the memory array to the data register. The Random Data Read (05h-E0h) command can be used to change the read address from the cache register.

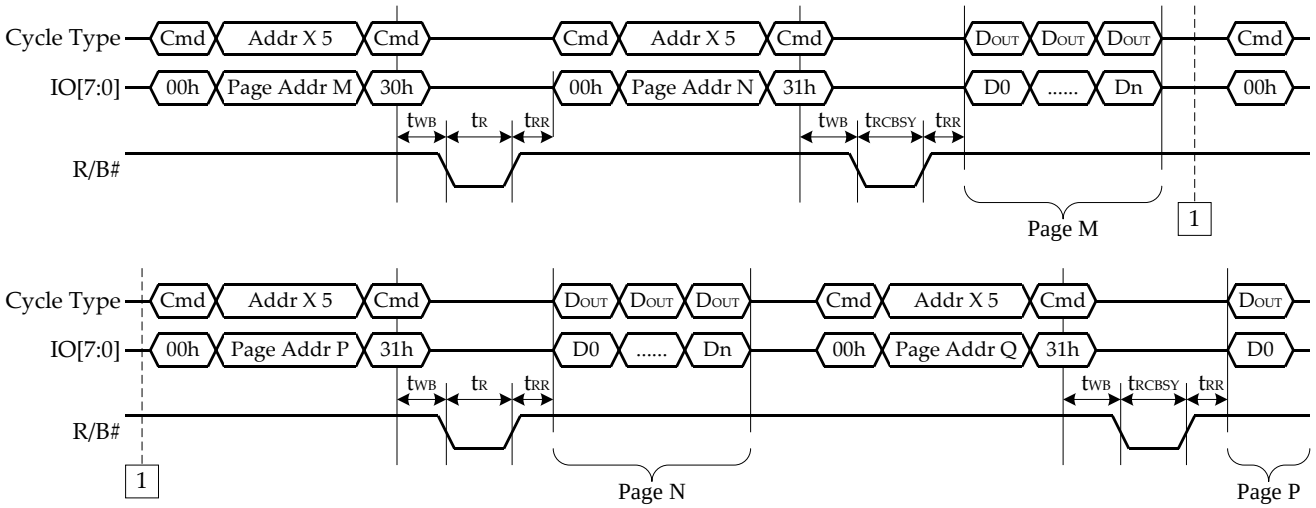

Figure 38: Read Page Cache Random Operation

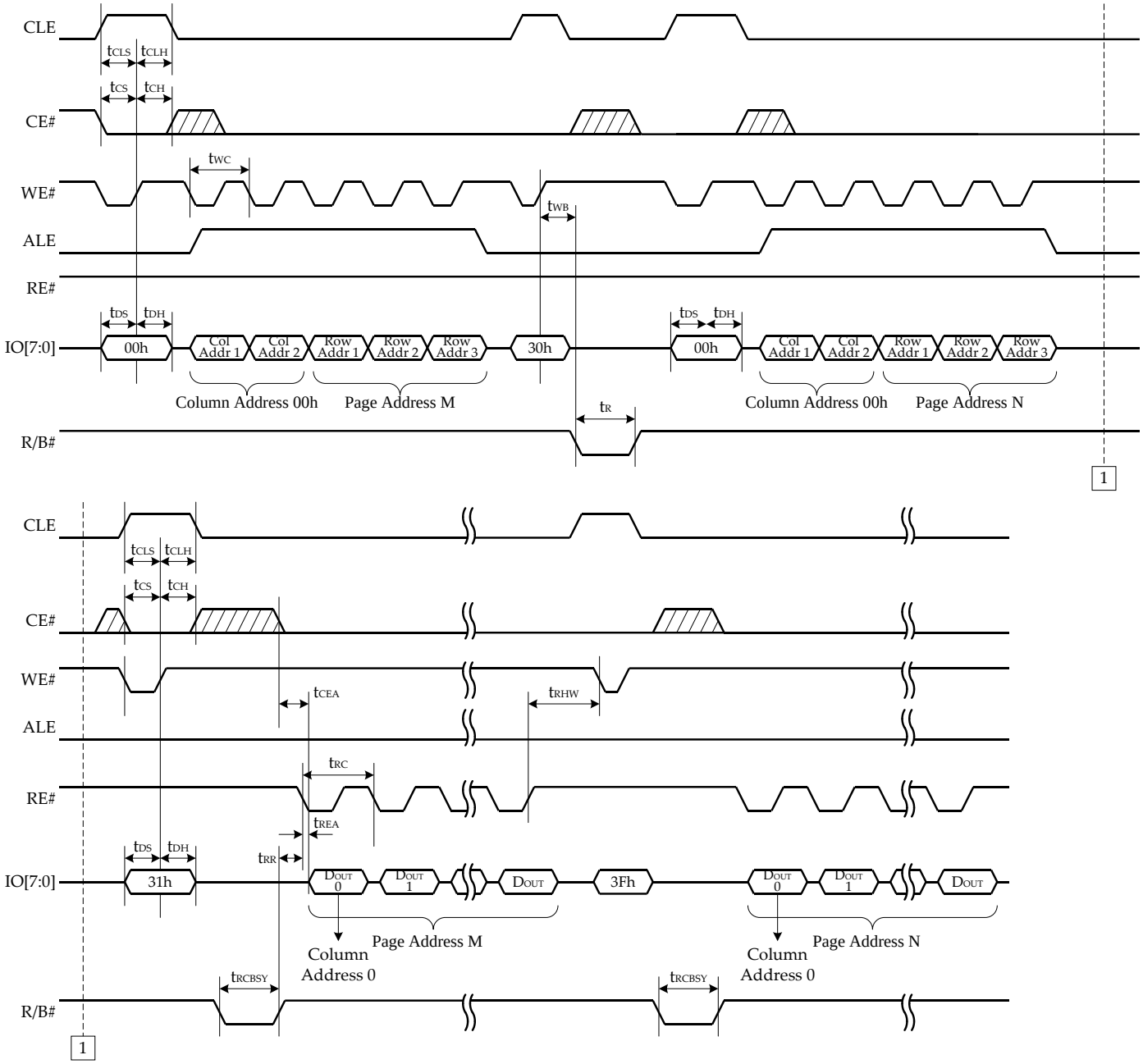

Figure 39: Read Page Cache Random Timing Diagram

4.8.5.Read Page Cache Last (3Fh)

The Read Page Cache Last (3Fh) command terminates the read page cache process and copies the page data from data register to cache register. This command is accepted by the die (LUN) when it is ready (RDY=1, ARDY=1) or during Read Page Cache (31h, 00h-31h) operations (RDY=1, ARDY=0).

After the 3Fh command is issued, R/B# goes low for t_{RCBSY} and the die (LUN) is busy (RDY=0, ARDY=0). After R/B# goes high, the status of the die (LUN) becomes ready (RDY=1, ARDY=1), which indicates the cache register is available for data output. The Random Data Read (05h-E0h) command can be used to change the read address from the cache register.

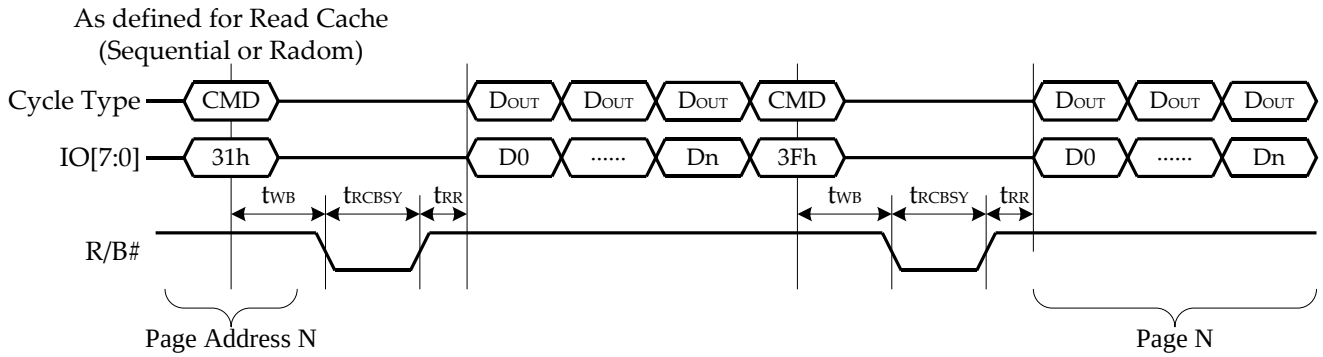

Figure 40: Read Page Cache Last (3Fh) Operation

4.9. Program Operations

Program operations loads data into the device, and moves data from cache register or data register to NAND Flash array via non-volatile programming process. The device is typically programmed in units of pages.

The host can monitor the device's R/B# pin to detect completion of the Program process, and Status Register should be polled to check the status of FAIL bit after Program completes.

Pages within a block should be sequentially programmed, starting from the least significant page address.

4.9.1. Program Page (80h-10h)

The Program Page (80h-10h) command accepts input data to the cache register, and writes data to the array page address specified in address cycles. This command is accepted by the die (LUN) when it is ready (RDY=1, ARDY=1) or during Program Page Cache (80h-15h) operations (RDY=1, ARDY=0).

The Program Page operation begins with 80h command and 5 address cycles, followed by data input cycles. After input data sequence is complete, 10h command initiates the program operation.

After the 10h command is issued, R/B# is driven low and the selected LUN goes busy (RDY=0, ARDY=0) for t_{PROG} (without internal ECC) or t_{PROG_ECC} (with internal ECC). The host can poll R/B# or status register (70h, 78h) for the completion of the process. After the die (LUN) returns to ready (RDY=1, ARDY=1) state, the host should check the FAIL bit in SR.

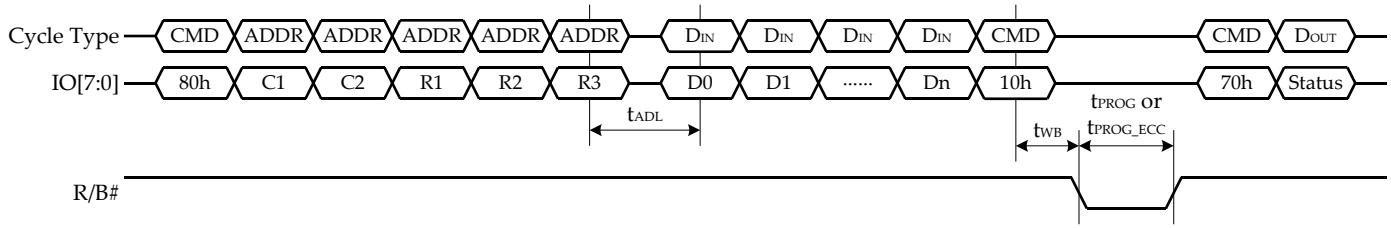

Figure 41: Program Page Operation

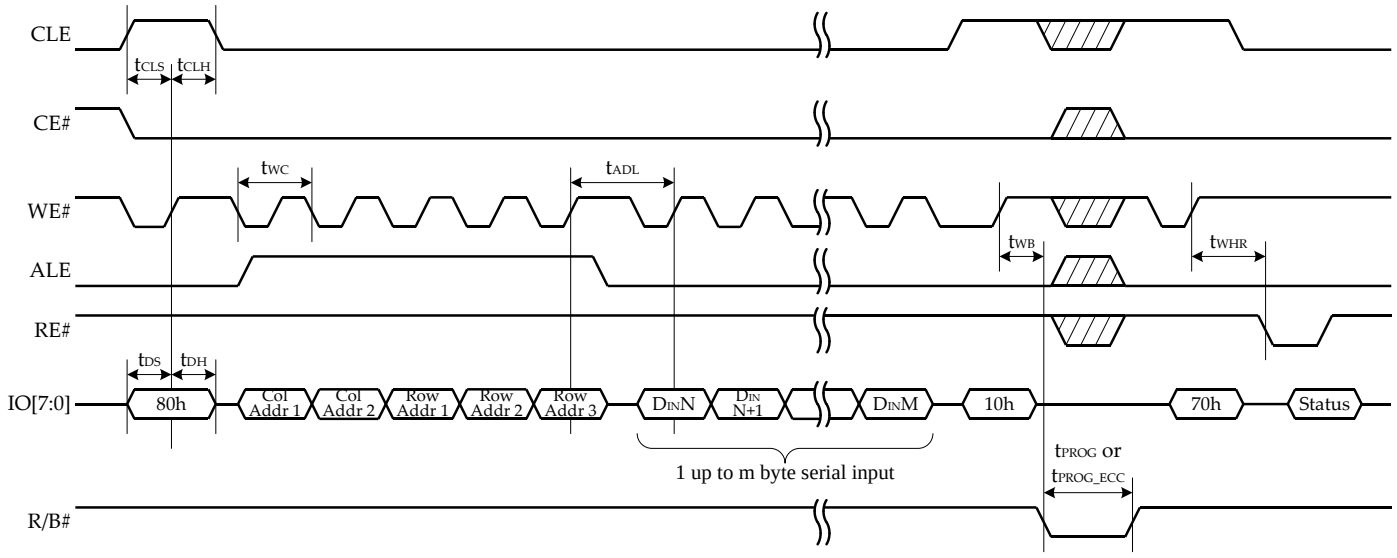

Figure 42: Program Page Timing Diagram

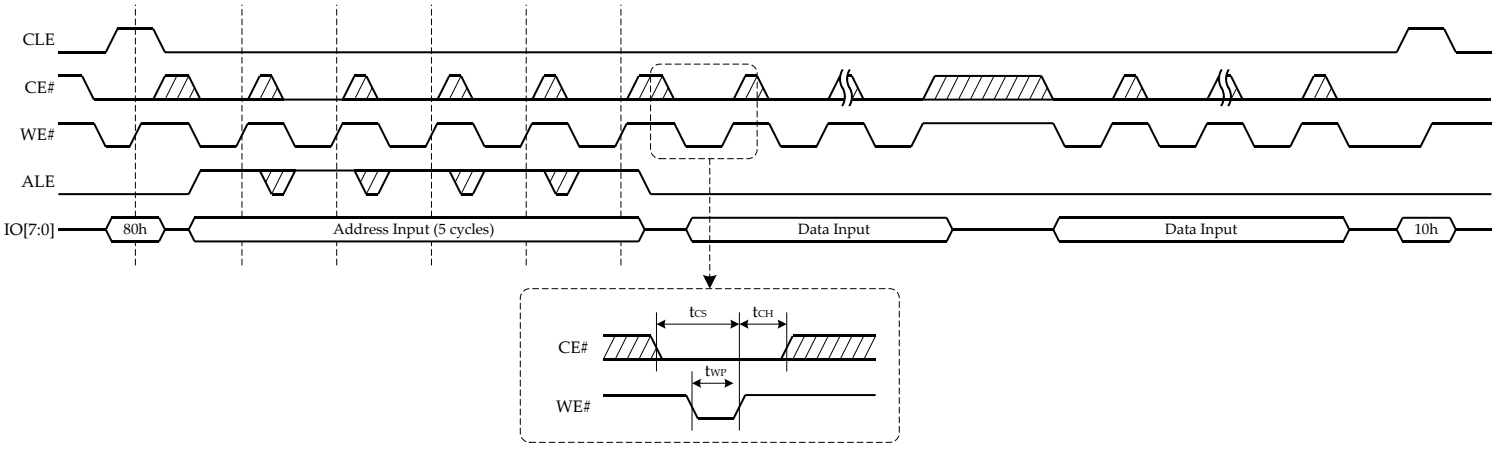

Figure 43: Program Page with CE# "Don't Care" Timing Diagram

4.9.2.Program Page Cache (80h-15h)

The Program Page Cache (80h-15h) command accepts input data to the cache register, copies it to the data register, and finally moves it to the memory array at the specified address of the selected die (LUN). After the data is copied to data register, the cache register is available for new data from Program Page Cache (80h-15h) or Program Page (80h-10h) commands. This command is accepted by the die (LUN) when it is ready (RDY=1, ARDY=1) or during Program Page Cache (80h-15h) operations (RDY=1, ARDY=0).

The Program Page Cache operation begins with a 80h command and 5 address cycles, followed by data input cycles and 15h command.

After the 15h command is issued, R/B# is driven low and the selected LUN goes busy (RDY=0, ARDY=0) for t_{CBSY} to perform internal operations. The host can poll R/B# or status register (70h, 78h) for the completion of the process. After the die (LUN) returns to busy with Program Cache operation (RDY=1, ARDY=0), the host should check the FAILC bit in SR.

Multiple 80h-15h commands can be cascaded in a series of commands; the host may use Program Page Cache (80h-10h) as the final command cycle. However, it is also acceptable to use 80h-15h without 80h-10h at the end; in such case, after t_{CBSY} the host should first poll the SR until ARDY=1, and then check FAIL and FAILC bits.

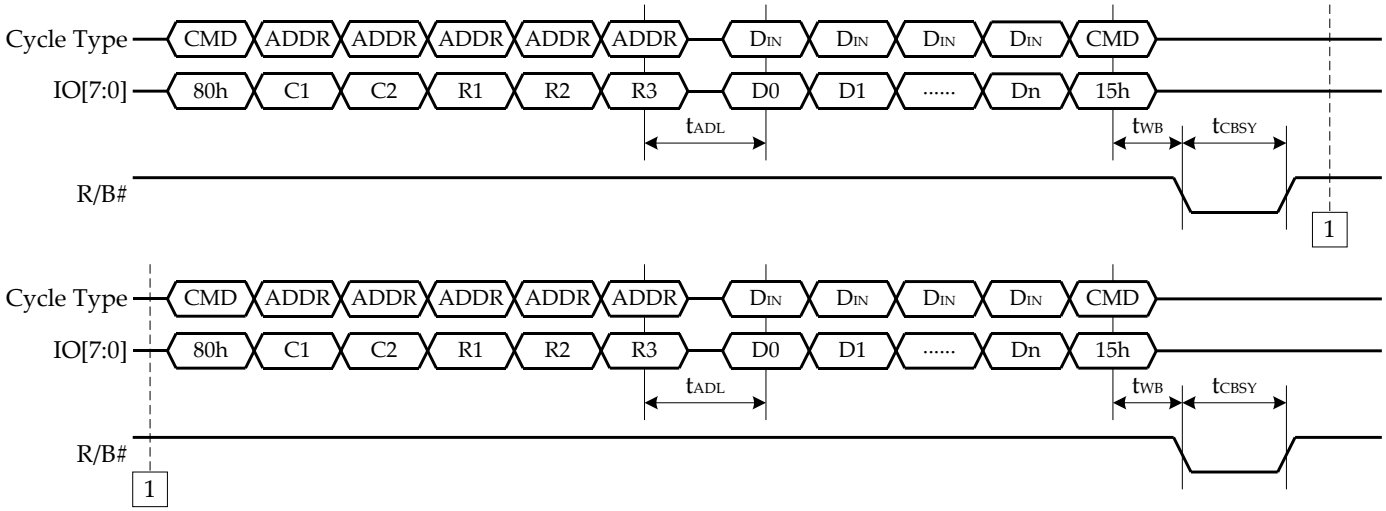

Figure 44: Program Page Cache (80h-15h) Operation (Start)

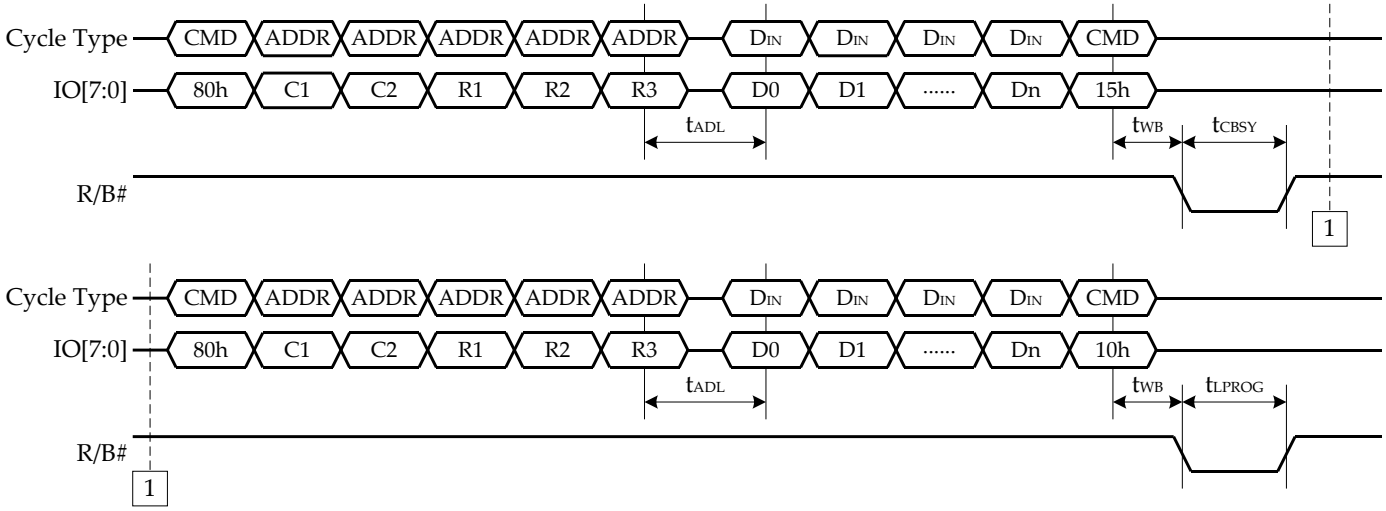

Figure 45: Program Page Cache (80h-15h) Operation (End)

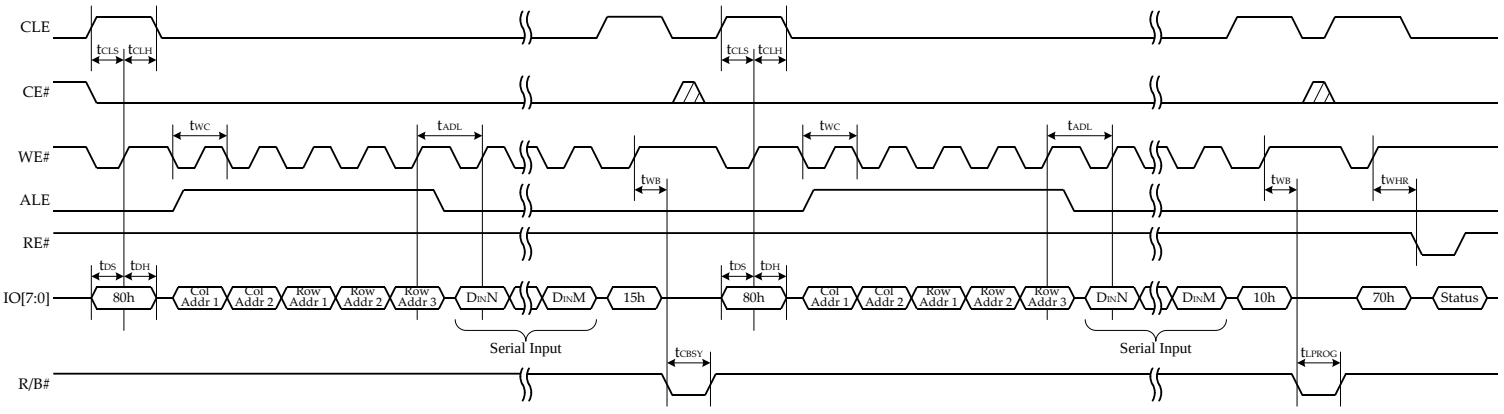

Figure 46: Program Page Cache Timing Diagram

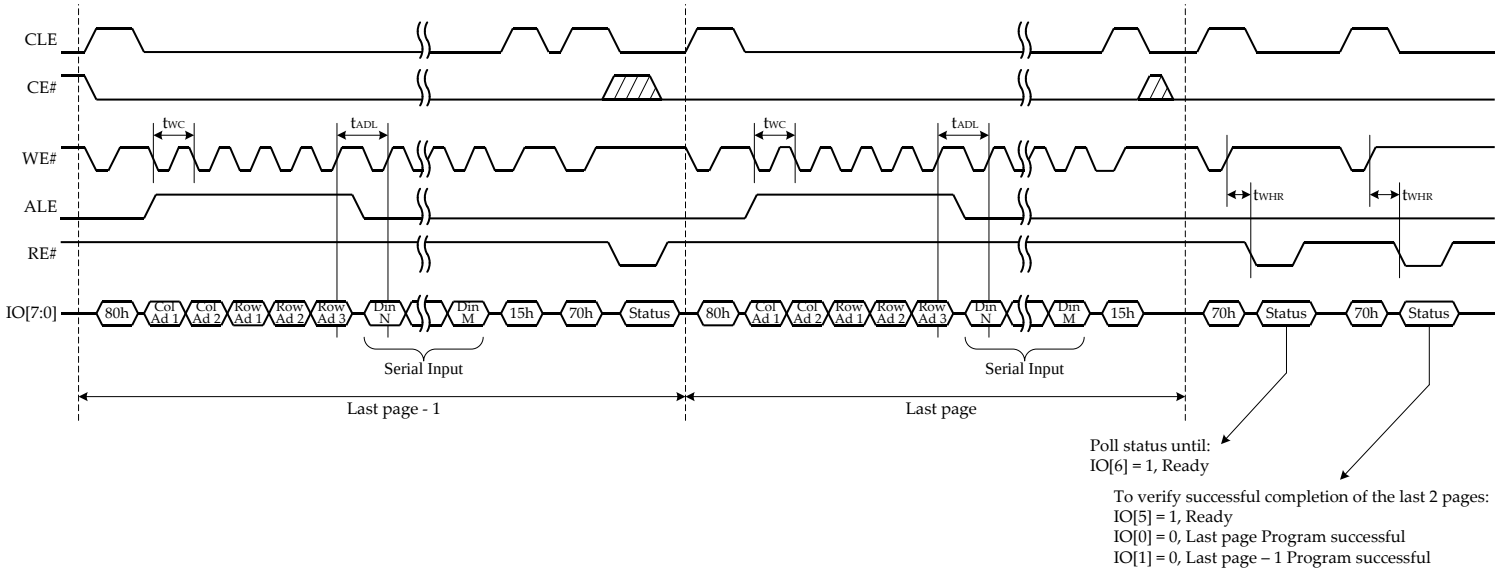

Figure 47: Program Page Cache Ending on 15h

4.9.3.Program Page Two-Plane (80h-11h)

The Program Page Two-Plane (80h-11h) command addresses a specific plane, accepts input data to its cache register, and queues it to be later programmed into the memory array. This command can be repeated to input data to specific planes and queue them for program operations. The Program Page (80h-10h) or Program Page Cache (80h-15h) command feeds data into the last plane and initiates the program operation of all queued planes. This commanded is accepted by the die (LUN) when it is ready (RDY=1).

The Program Page Two-Plane (80h-11h) command begins with an 80h command and 5 address cycles, followed by data input cycles and 11h command.

After the 11h command is issued, R/B# is driven low and the selected LUN goes busy (RDY=0, ARDY=0) for t_{CBSY} to perform internal operations. The host can poll R/B# or status register (70h, 78h) for the completion of the process. After the die (LUN) returns to ready (RDY=1), additional 80h-11h, 80h-10h or 80h-15h commands can be issued.

If Program Page (80h-10h) is used as the final command, the die (LUN) will go busy for t_{PROG}. After it returns to ready (RDY=1, ARDY=1), the host should check the SR for FAIL bit of all planes to confirm the status of program operation.

If Program Page Cache (80h-15h) is used as the final command, the die (LUN) will go busy for t_{CBSY}. After it returns to ready, the host should check the SR for FAILC bit of all planes to confirm the status of program operation.

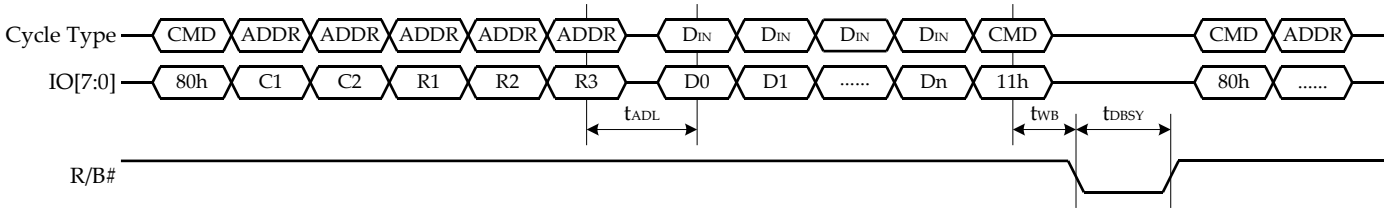

Figure 48: Program Page Two-Plane (80h-11h) Operation

4.10. Erase Operations

NAND Flash devices are erased on a block basis. All data bytes in the block are cleared to FFh by erase operation. An erased block is ready for program operations.

4.10.1. Erase Block (60h-D0h)

The Erase Block (60h-D0h) command erases the addressed block. This command is accepted by the die (LUN) when it is ready (RDY=1, ARDY=1).

The Erase Block operation begins with a 60h command and three address cycles, followed by D0h command which starts the erase process.

After the D0h command is issued, R/B# is driven low and the selected LUN goes busy (RDY=0, ARDY=0) for t_{BERS} while erase operation is in progress. The host can poll R/B# or status register (70h, 78h) for the completion of the process. After the die (LUN) returns to ready (RDY=1, ARDY=1) state, the host should check the FAIL bit in SR.

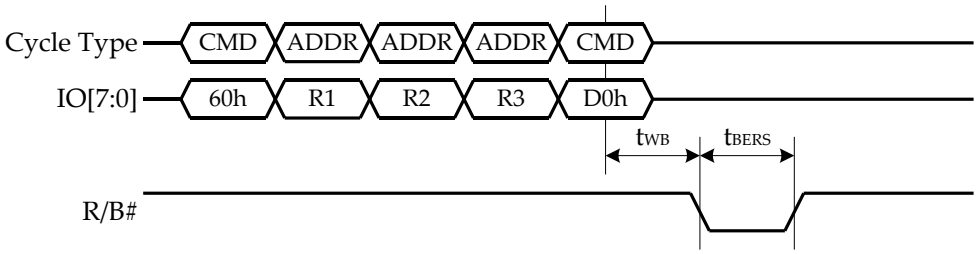

Figure 49: Erase Block Operation

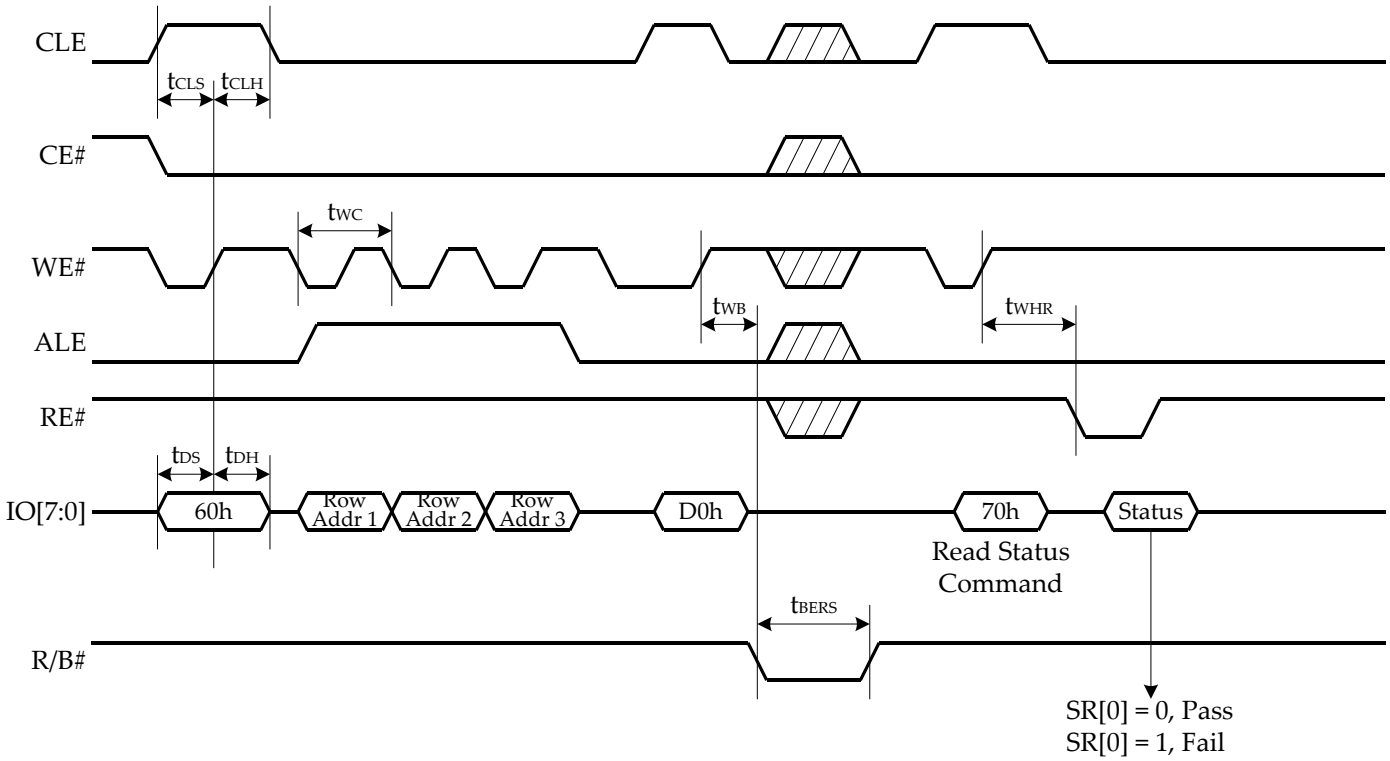

Figure 50: Erase Block Timing Diagram

4.10.2. Erase Block Two-Plane (60h-D1h) Operation

The Erase Block Two-Plane (60h-D1h) command addresses a specific block and queues it to be later erased. This command can be repeated to queue specific blocks for erase operations. The Erase Block (60h-D0h) command feeds the address of the final block and initiates the Erase operation for all blocks in the queue. This command is accepted by the die (LUN) when it is ready (RDY=1, ARDY=1).

The operation begins with a 60h command and three row address cycles, followed by D1h command. The page address is ignored.

After D1h command is issued, R/B# is driven low and the selected LUN goes busy (RDY=0, ARDY=0) for t_{DBSY} to

perform internal operations. The host can poll R/B# or status register (70h, 78h) for the completion of the process. After the die (LUN) returns to ready (RDY=1, ARDY=1) state, additional 60h-D1h or 60h-D0h commands can be issued.

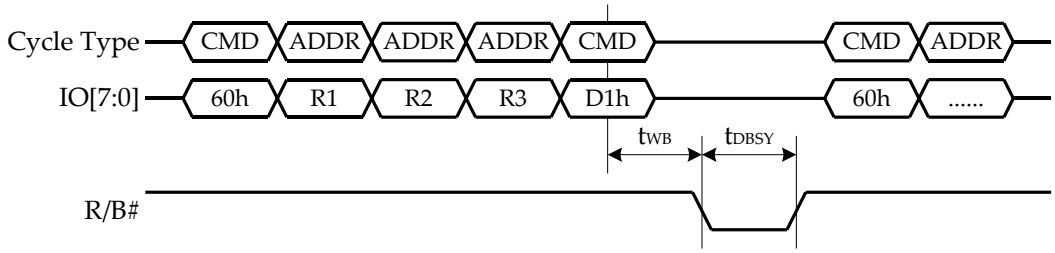

Figure 51: Erase Block Two-Plane (60h-D1h) Operation

4.11. Internal Data Move Operations

Internal data move operations take advantage of cache register and internally transfers data from one page to another page in the memory array, without the use of an external memory. This mechanism simplifies host operations when moving data between the pages is required, and is especially useful when performing bad block management and wear leveling.

To implement internal data move, first use the Read For Internal Data Move (00h-35h) command to copy the address page from memory array to the cache register, and then issue the Program For Internal Data Move (85h-10h) command to write the data to a new address in the memory array.

Following commands are accepted between 00h-35h and 85h-10h commands: status operations (70h, 78h), column address operations (05h-E0h, 06h-E0h, 85h). Interleaved die (multi-LUN) operations are prohibited between 00h-35h and 85h-10h.

Internal data move operations cannot cross plane or die (LUN) boundaries. To move data to a new plane or a new die (LUN), it is up to the host to first read the data out of the device, and then program it back to the expected address.

4.11.1. Read For Internal Data Move (00h-35h)

The Read For Internal Data Move (00h-35h) command is functionally equivalent to the Read Page (00h-30h) command. It copies a page from the array to the cache register and enables data output.

After 00h-35h command, R/B# of the selected die (LUN) is pulsed low for t_R during internal operations. When the device is ready (RDY=1, ARDY=1) again, upcoming commands can be issued.

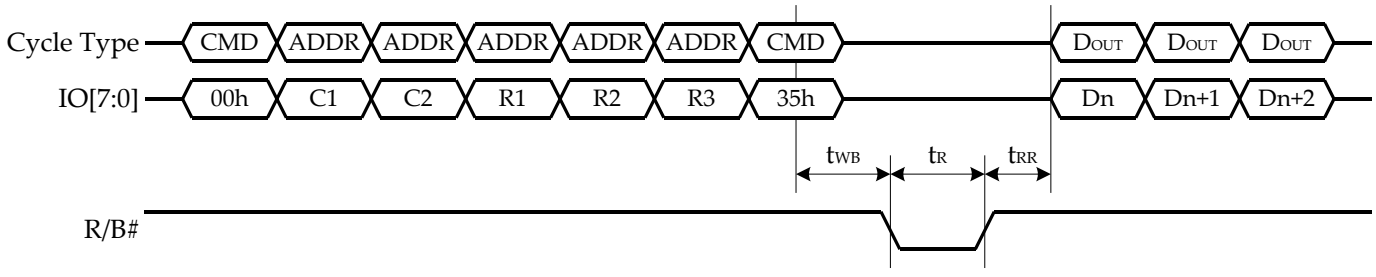

Figure 52: Read For Internal Data Move (00h-35h) Operation

During internal data move operations, after 00h-35h moves page data to cache register and the device returns to ready state, the host can output data using Random Data Read (05h-E0h) command.

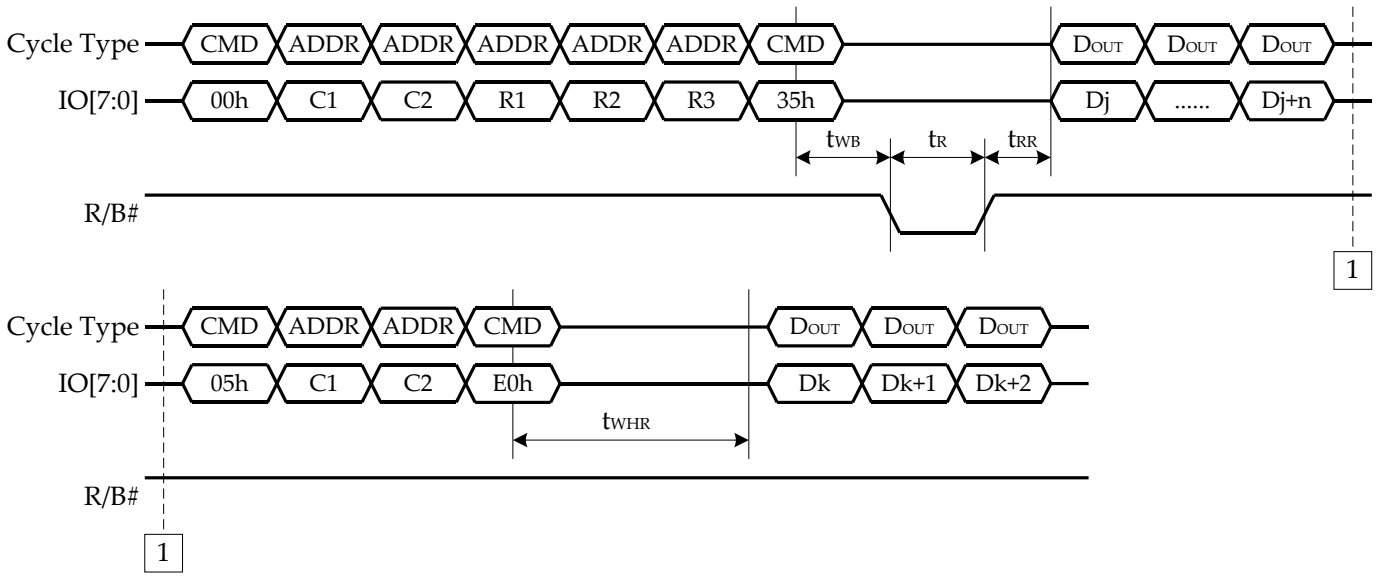

Figure 53: Read For Internal Data Move (00h-35h) with Random Data Read (05h-E0h)

4.11.2. Program For Internal Data Move (85h-10h)

The Program For Internal Data Move (85h-10h) command is functionally equivalent to the Program Page (80h-10h) command, except that the cache register is not cleared. This command programs a page to the designated memory array address.

After 85h-10h command, R/B# of the selected die (LUN) is pulsed low for t_{PROG} during internal operations. When the device is ready (RDY=1, ARDY=1) again, the host should check the FAIL bit in SR.

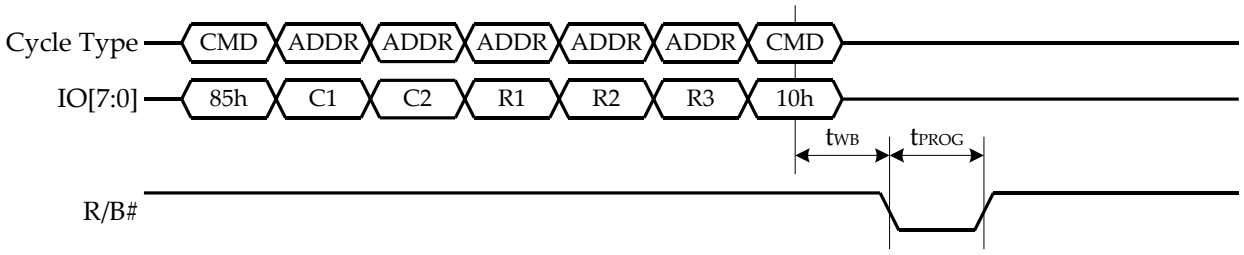

Figure 54: Program for Internal Data Move (85h-10h) Operation

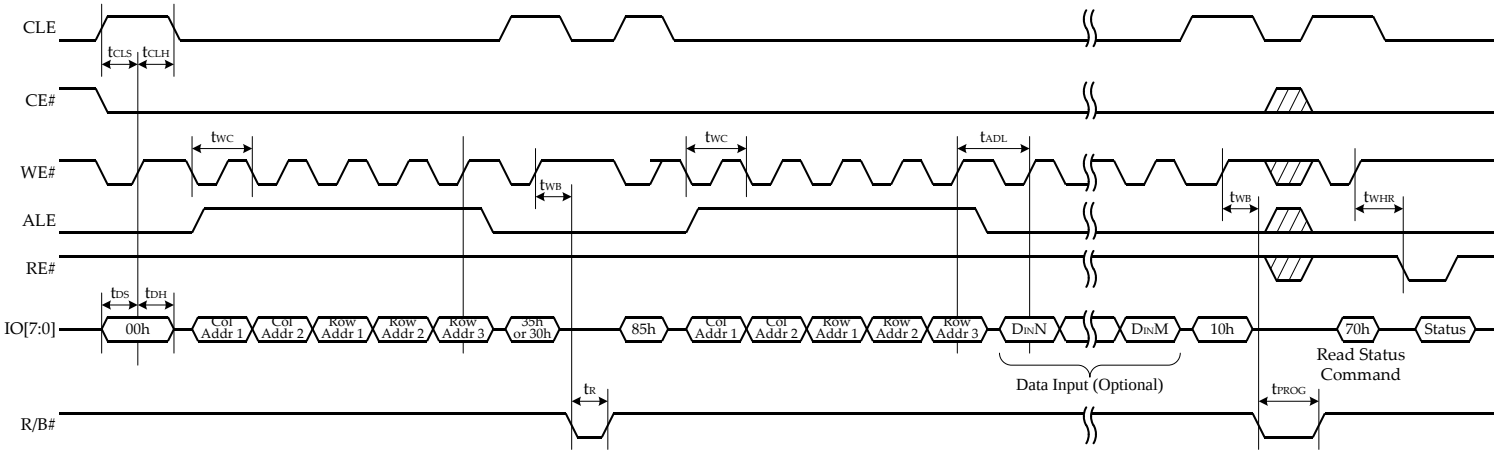

Figure 55: Internal Data Move Timing Diagram

While the 85h-10h command is in progress, the Program For Internal Data Input (85h) command can be issued to change the program address.

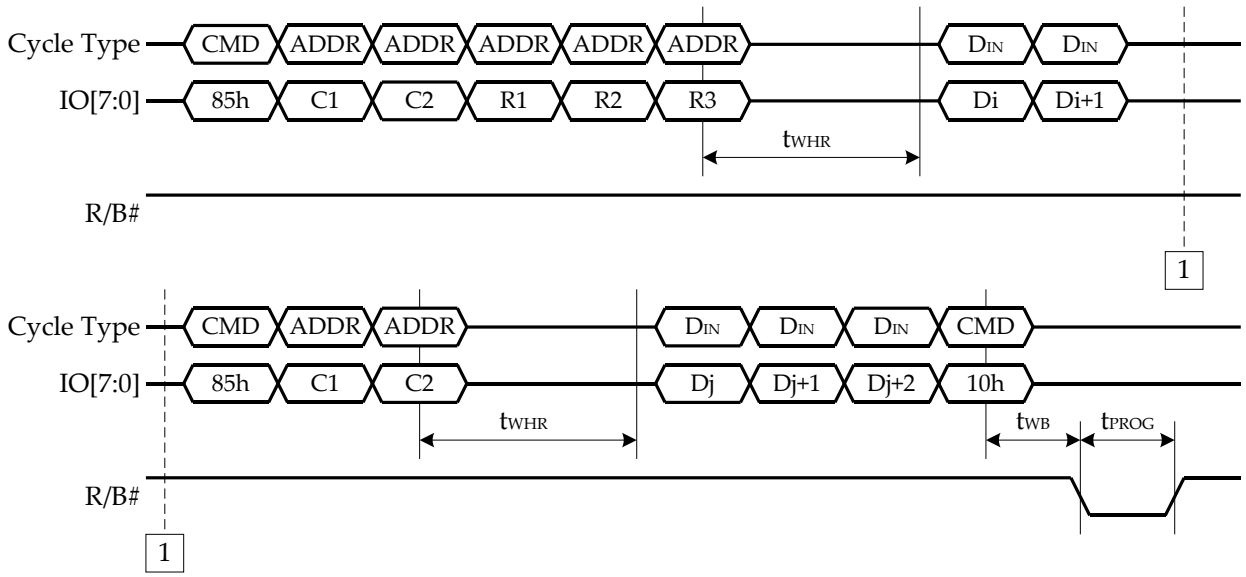

Figure 56: Program for Internal Data Move (85h-10h) with Random Data Input (85h)

4.11.3. ECC Concerns in Internal Data Move Operations

To ensure data integrity, it is recommended to read data out of the device and check for ECC errors after the 00h-35h command, so that corrected data can be used with 85h-10h command. However, if internal ECC is enabled, then chip internal logic can handle ECC verification and data correction without host intervention, thus improving system performance.

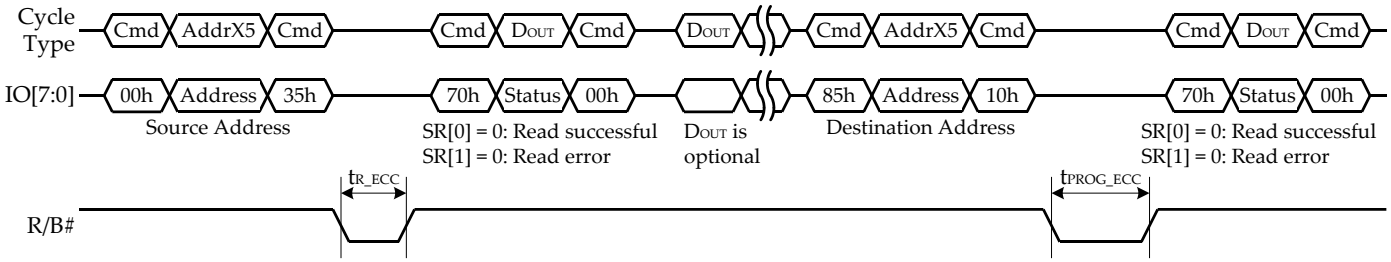

Figure 57: Internal Data Move (85h-10h) with Internal ECC Enabled

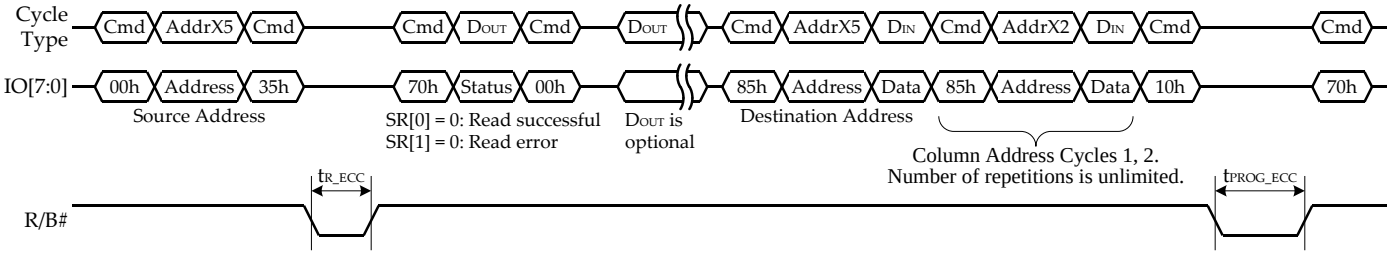

Figure 58: Internal Data Move (85h-10h) with Random Data Input with Internal ECC Enabled

4.12. Block Lock Feature

Block lock feature allows a specific range of blocks of the device to be protected against program and erase operations.

4.12.1. Unlock (23h, 24h)

The Unlock (23h, 24h) commands select a range of blocks for program or erase operations. The 23h command specifies the lower boundary block address register, while 24h specifies the upper boundary block address. The

LSB of the page address corresponds to the invert area bit.

The device allows only one range of blocks to be specified. If Unlock (23h, 24h) commands are issued many times, then previous address values are lost and only the latest command takes effect.

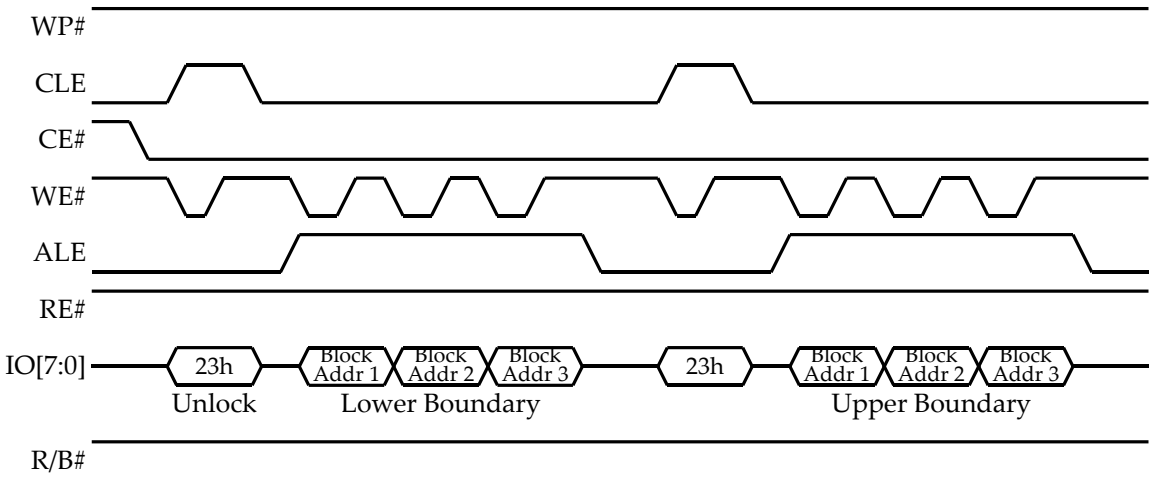

Figure 59: Unlock Operations

4.12.2. Lock (2Ah)

The Lock (2Ah) command locks all blocks of the device. If there are blocks previously unlocked by 23h and 24h commands, then the Lock (2Ah) command will lock them, protecting these blocks against program and erase operations.

If Lock pin is Low at power-up, or if the device is locked tight, then the Lock (2Ah) command will not take effect.

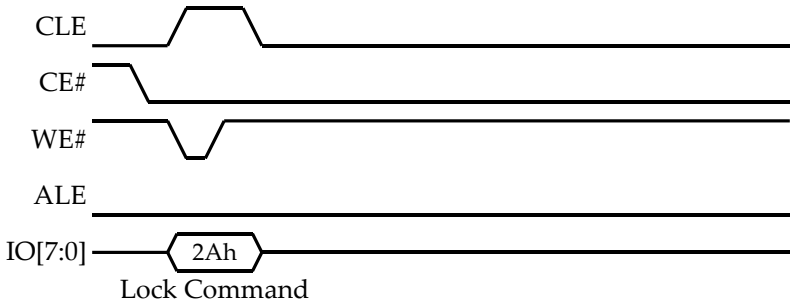

Figure 60: Lock Operation

4.12.2.1. Effect On Program Or Erase Operations

If Program or Erase operation is attempted on a locked block address, then R/B# goes Low for t_{LBSY} and the program or erase operation is not executed. Polling status register will return SR[7] = 0, indicating the protect status of the block.

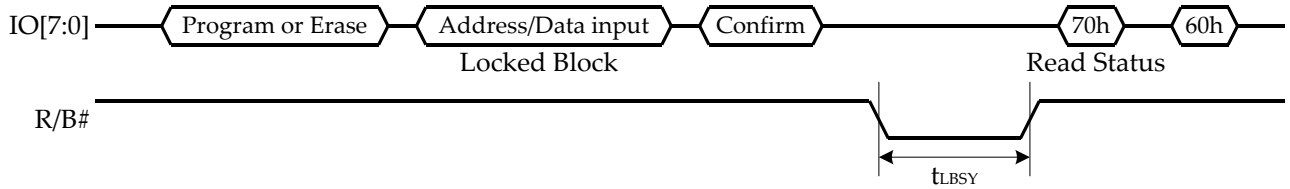

Figure 61: Program/Erase Command Issued to Locked Block

4.12.3. Lock Tight (2Ch)

The Lock Tight (2Ch) command prevents the block lock/unlock status to be changed. When WP# pin is High and Lock Tight (2Ch) command is issued, all Unlock (23h) and Lock (2Ah) commands are disabled, offering an extra level of protection mechanism that prevents programming or erasing operations on locked blocks.

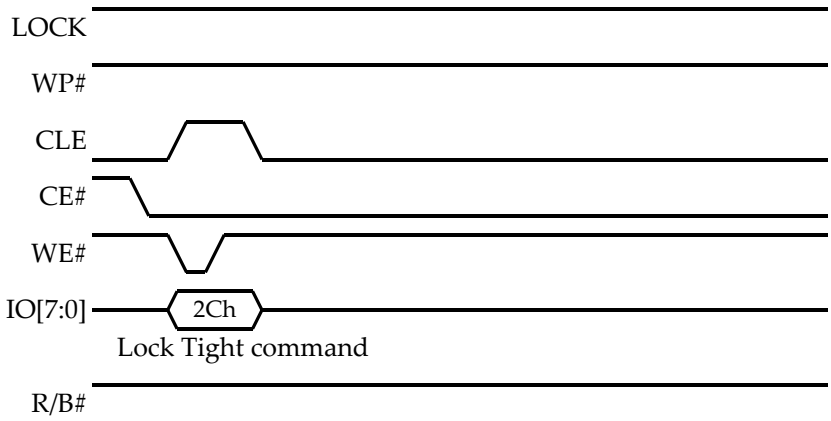

Figure 62: Lock Tight Operation

4.12.3.1. Effect On Program And Erase Operations

If Program or Erase operation is attempted on a locked block address that is also locked tight, then R/B# goes Low for t_{LBSY} and the program or erase operation is not executed. Polling status register will return SR[7] = 0, indicating the protect status of the block.

If Program or Erase is performed on unlocked blocks after Lock Tight command is issued, then the program or erase operation can be successfully completed.

4.12.3.2. Disabling Lock Tight

After the Lock Tight command is issued, it cannot be disabled using software command. It can be disabled by:

1. Power cycling the device;
2. Toggling WP# pin.

After the lock tight status is disabled, all blocks will become locked. It has the same effect as Lock (2Ah) command.

The execution of Lock Tight (2Ch) command is disabled if LOCK pin is Low at device power-up.

4.12.4. Block Lock Read Status (7Ah)

The Block Lock Read Status (7Ah) command accesses the Block Lock Status Register and returns the protection status of a specified block.

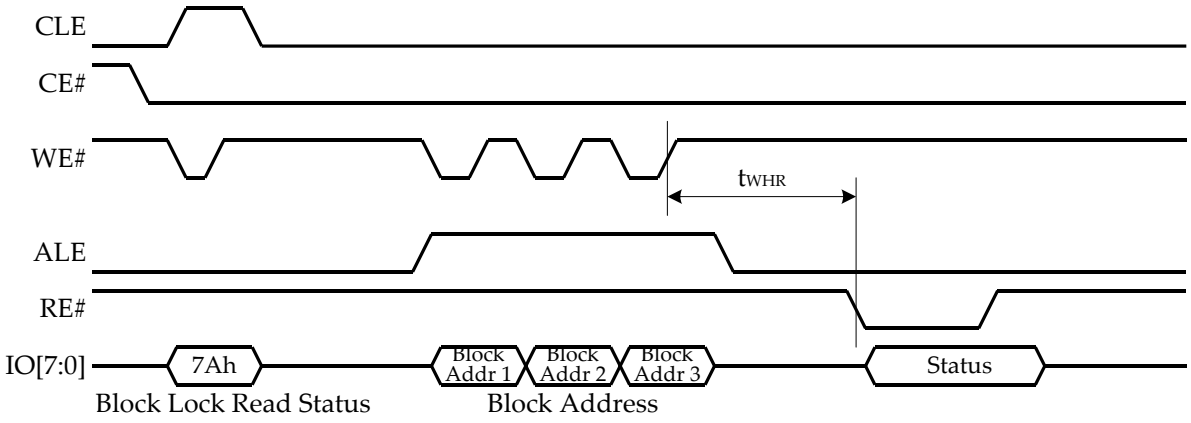

Figure 63: Block Lock Read Status

4.13. One-Time Programmable (OTP) Operations

The device has a built-in one-time-programmable (OTP) address space with 30 pages (2112 bytes for each page)

for non-erasable storage purposes. The page address space of OTP area is 02h - 1Fh.

OTP area is accessible to the user only when the device is in OTP operation mode. To enable OTP operation mode, the Set Feature (EFh) command should be issued to feature address 90h, and write 01h, 00h, 00h, 00h to P1, P2, P3, P4, respectively. For more OTP-related settings, see "2.9 Device Feature Table" for details.

While the device is in OTP operation mode, Page Read (00h-30h) and Program Page (80h-10h) commands can be issued to OTP area for read or program operations. OTP area allows up to eight partial-page program operations for a given page, while other blocks allow only four partial-page program operations.

OTP area cannot be erased, regardless of its protection status.

4.13.1. Legacy OTP Commands

For compatibility considerations, refer to appropriate datasheet for the definitions of OTP Data Program (A0h-10h), OTP Data Protect (A5h-10h) and OTP Data Read (AFh-30h) commands.

4.13.2. OTP Data Program (80h-10h)

The OTP Data Program (80h-10h) command writes data to a specified page in OTP area. A page in OTP area can either be programmed in one time, or partially programmed for up to eight times. The OTP pages should be programmed in ascending order.

This command is compatible with the Random Data Input (85h) command, and it allows to program to an offset of the OTP page with two bytes of column address (CA[12:0]). This command takes no effect if the OTP area is protected.

To program an OTP page, the Program Page command begins with 80h command, followed by two cycles of column address and address cycles that select a specific page within a range of 02h-00h through 1Fh-00h. Data input cycles may contain 1 to 2112 bytes. After input data sequence is complete, 10h command initiates the program operation.

After the 10h command is issued, R/B# is driven Low and the device goes busy for t_{PROG}. To access the status register while the device is in OTP mode, only Read Status (70h) command is applicable. The state of R/B# pin is reflected by SR[5]. After the device is ready, the host should check the FAIL bit of SR.

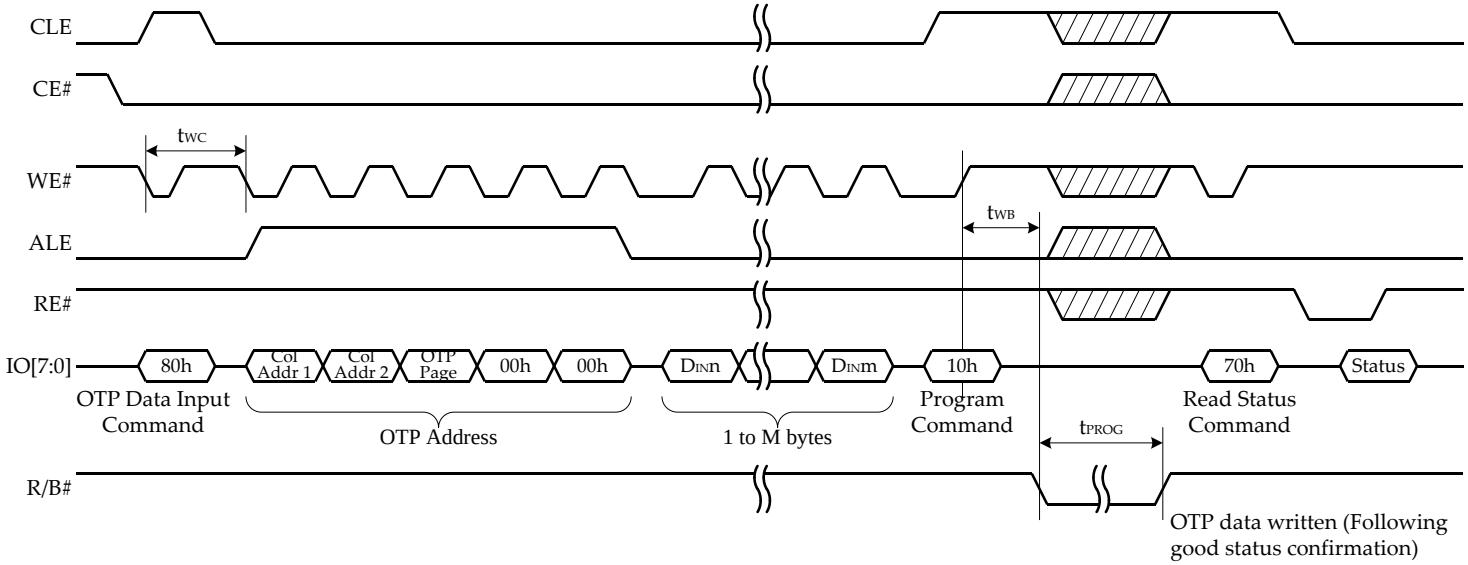

Figure 64: OTP Data Program Operation (After Entering OTP Operation Mode)

Notes:

1. The OTP Page address cycle must fall within the range of 02h-1Fh.
2. For x8 device, M=2112 bytes;
   for x16 device, M=1056 words.

4.13.3. Random Data Input (85h)

While programming an OTP page, during the data input cycles of 80h-10h commands, Random Data Input (85h) command allows the host to write additional data to a new column address. Within a specific page, the 85h command can be issued any number of times before the 10h command.

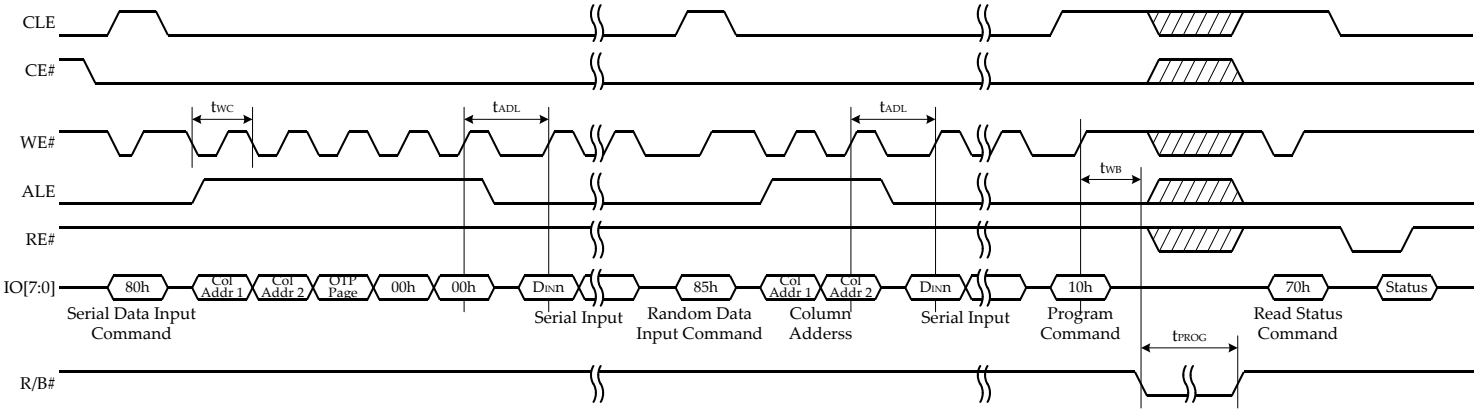

Figure 65: OTP Data Program Operation with Random Data Input (After Entering OTP Operation Mode)

4.13.4. OTP Data Protect

The OTP Data Protect (80h-10h) command protects the OTP area and prevents further program operations in the OTP area.

To protect the entire OTP area, first issue the 80h command, followed by column address fixed to 0, OTP protect page address, and block address fixed to 0. Then, write 00h data and issue 10h command.

After the 10h command is issued, R/B# is driven Low and the device goes busy for t_{PROG}. To access the status register while the device is in OTP mode, only Read Status (70h) command is applicable. The state of R/B# pin is reflected by RDY bit. After the device is ready, the host should check the FAIL bit of SR.

If OTP Data Protect command is issued when the OTP area is already protected, then R/B# goes Low for t_{OBSY}, and the status register becomes 60h after the device returns to ready state.

After data protection has taken effect, the entire OTP area is protected against program operations, and cannot be unprotected.

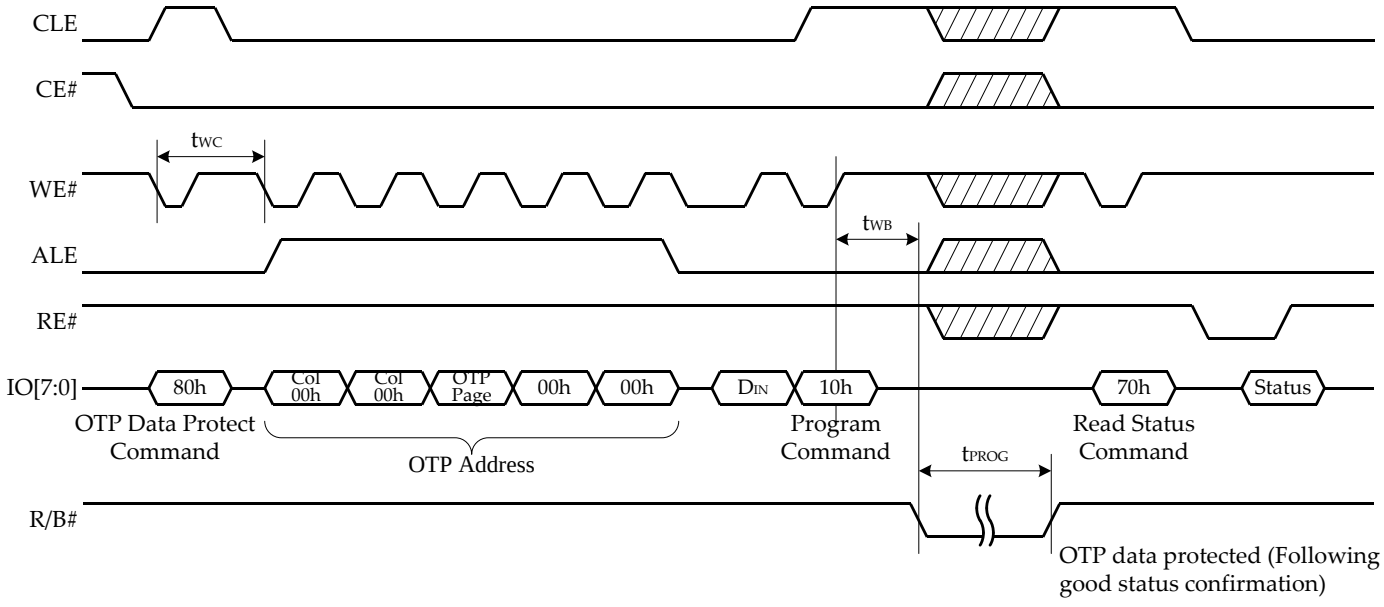

Figure 66: OTP Data Protect Operation (After Entering OTP Operation Mode)

4.13.5. OTP Page Read (00h-30h)

The OTP Page Read (00h-30h) command reads data in OTP area if the device is already in OTP operation mode. The OTP area can always be read, regardless of its protection status.

The OTP Page Read command begins with 00h command in combination with appropriate address cycles: first two cycles are the column address, while the latter three cycles specifies a page in the range of 02h-00h-00h and 1Fh-00h-00h. After address cycles are finished, issue the 30h command to launch the read operation. Only data in the currently addressed page is output in the read process.

The R/B# pin will go Low for t_R while the device is busy doing internal operations. To access the status register while the device is in OTP mode, only Read Status (70h) command is applicable. The state of R/B# pin is reflected by SR[5]. After the device is ready again, the host may drive data output by repetitively pulsing the RE# pin.

The host may select additional pages in the OTP area by issuing multiple OTP Data Read commands. Normal Read operation timings also apply to the OTP read process.

The Page Read Cache Mode command is not applicable for OTP operations.

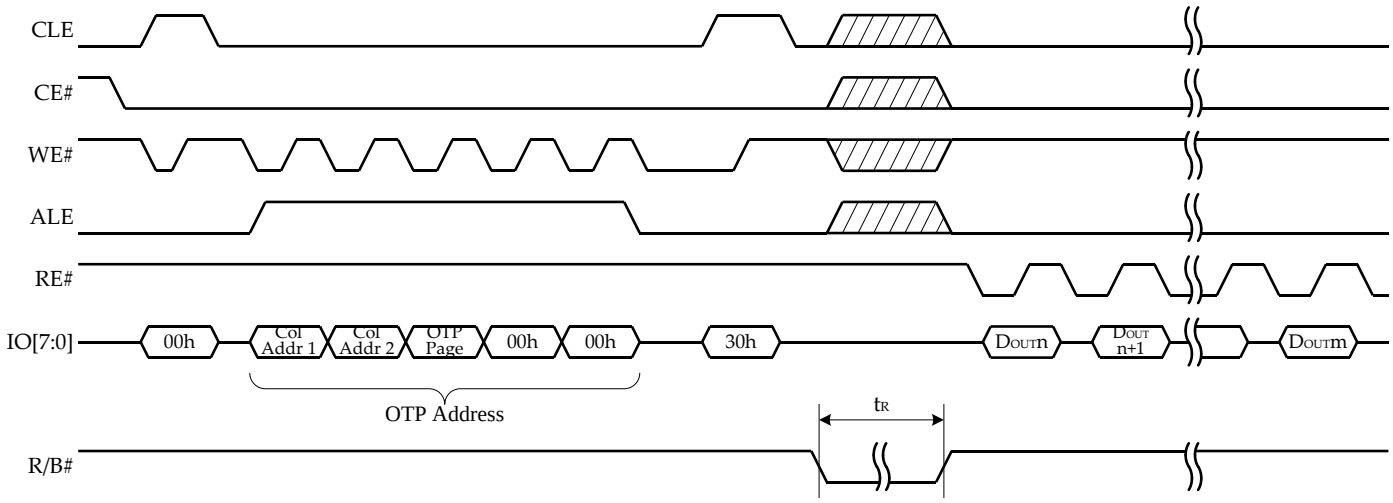

Figure 67: OTP Data Read Operation

Notes:

1. The OTP Page address cycle must fall within the range of 02h-1Fh.

The Page Read (00h-30h) command is compatible with the Random Data Output (05h-E0h) command. See the figure below for details.

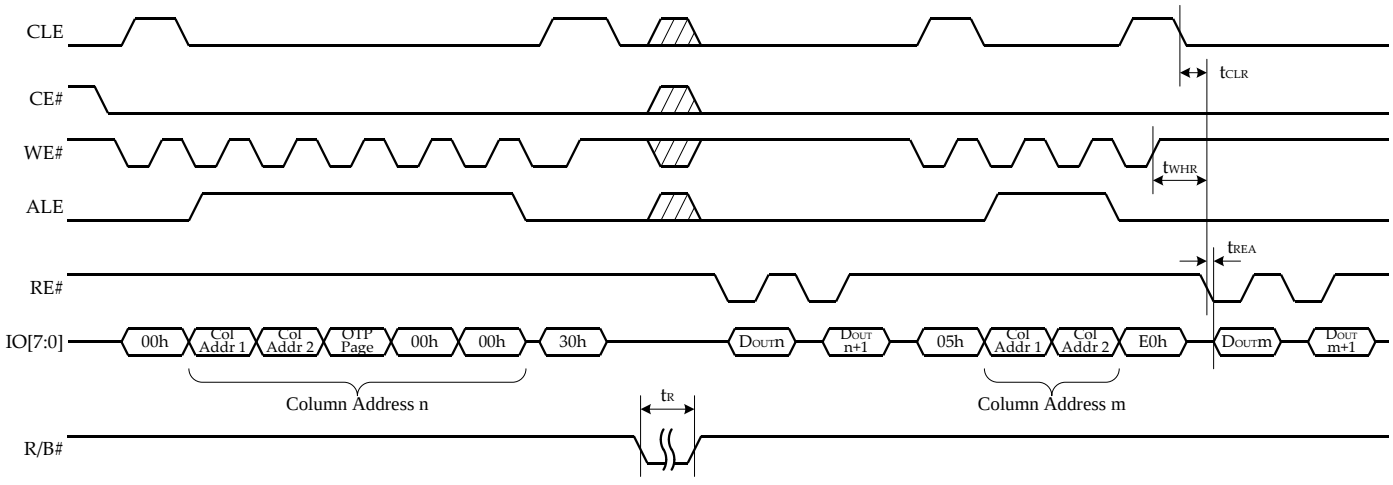

Figure 68: OTP Data Read with Random Data Read Operation

Notes:

1. The OTP Page address cycle must fall within the range of 02h-1Fh.

5. Two-Plane Operations

In the NAND Flash device, each LUN is further divided into multiple physical planes. A plane is addressed by the low-order block address bits.

Each plain contain its own cache register and data register. Two-plane operations take advantage of the device architecture and allow concurrent Read, Program or Erase operations on multiple planes, which significantly improve system performance. The two concurrent operations on two planes must be of the same type. As an example, programming one plane while erasing another is not possible.

After a Two-Plane Program Page or Erase Block operation is issued, the Read Status (70h) command should be issued to access the status register which indicates whether the previous operation(s) failed or succeeded; if FAIL=1 and/or FAILC=1, then the Read Status Enhanced (78h) command can be issued to further determine which plane has the error.

5.1. Two-Plane Addressing

For two-plane commands, each operational plane requires its own five-cycle address. The addresses for a two-plane operation should meet the following requirements:

1. The LUN address bit(s) should be identical for all addresses.
2. The BA[6] (plane selection) bit should be different for each address.
3. The PA[5:0] (page address) bits should be identical for each address.

5.2. Two-Plane Page Read

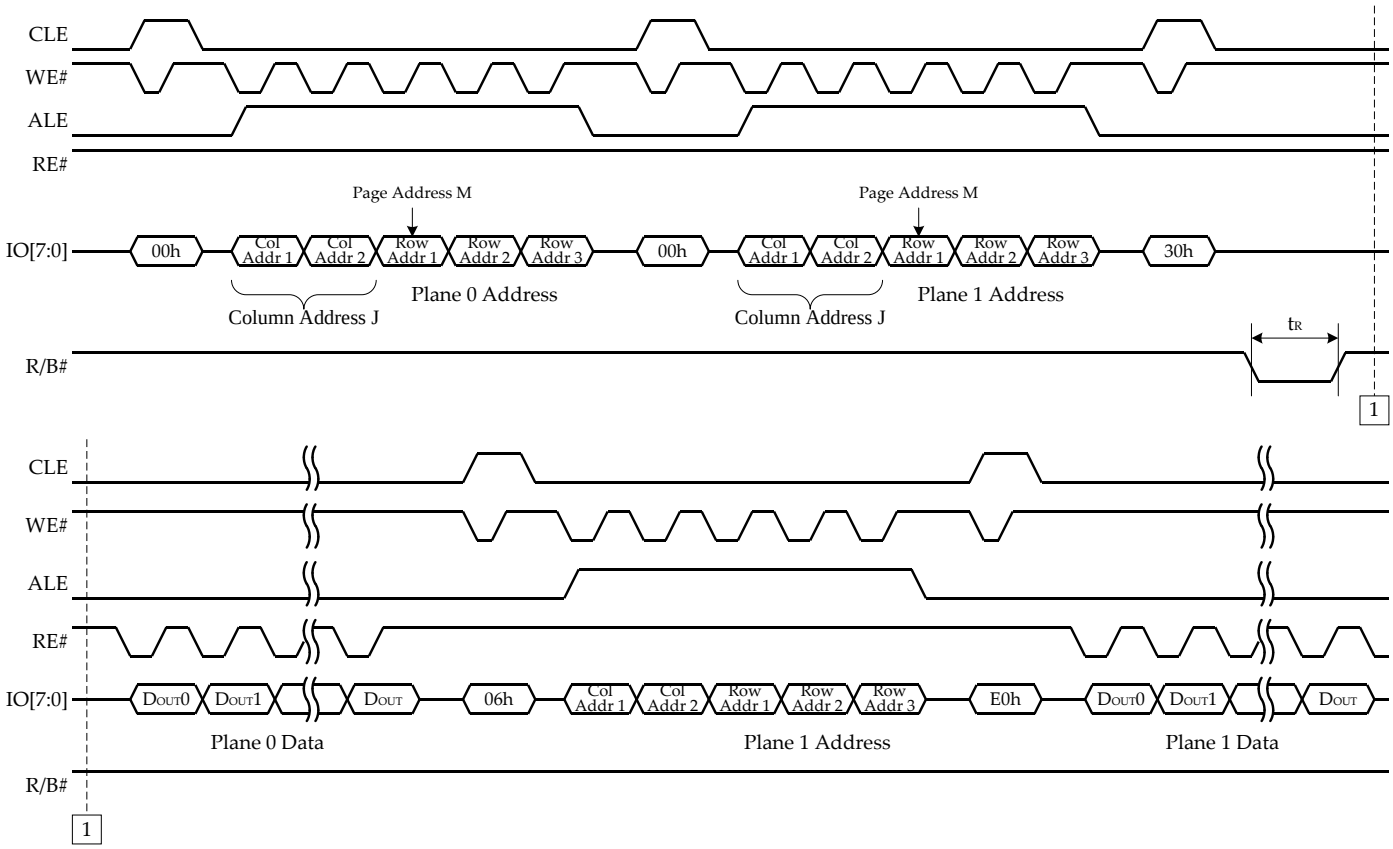

Figure 69: Two-Plane Page Read

Notes:

1. Column and page addresses should be identical for the two planes.

2. BA6 should be different for the two planes.

5.3. Two-Plane Page Read with Random Data Read

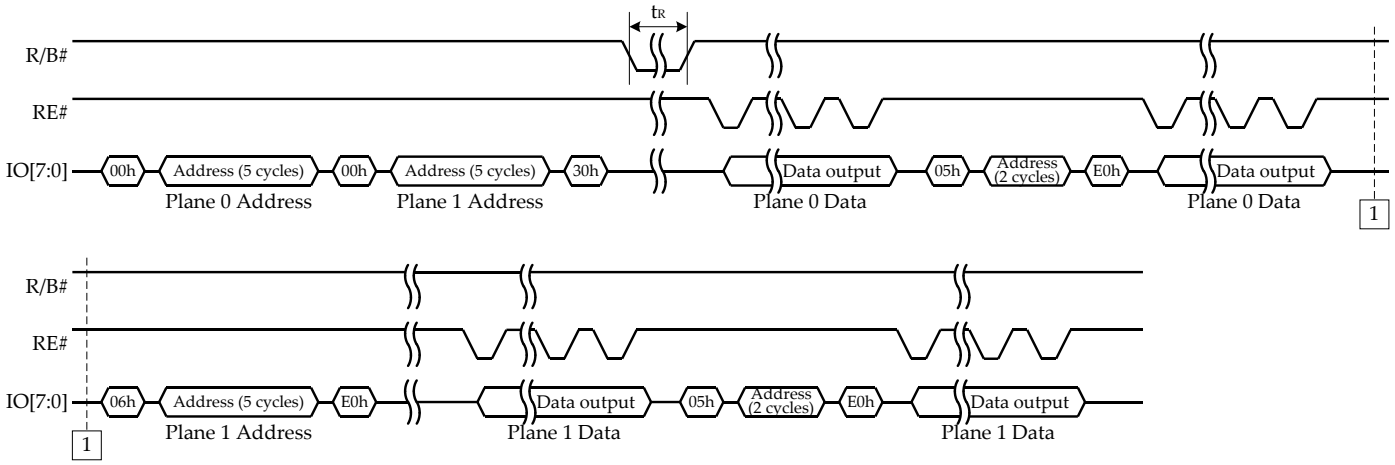

Figure 70: Two-Plane Page Read with Random Data Read

5.4. Two-Plane Program Page

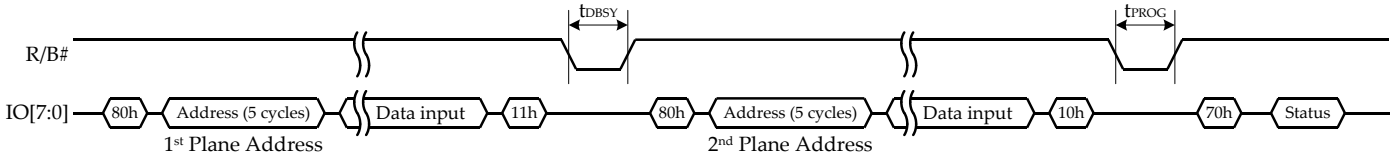

Figure 71: Two-Plane Program Page

5.5. Two-Plane Program Page with Random Data Input

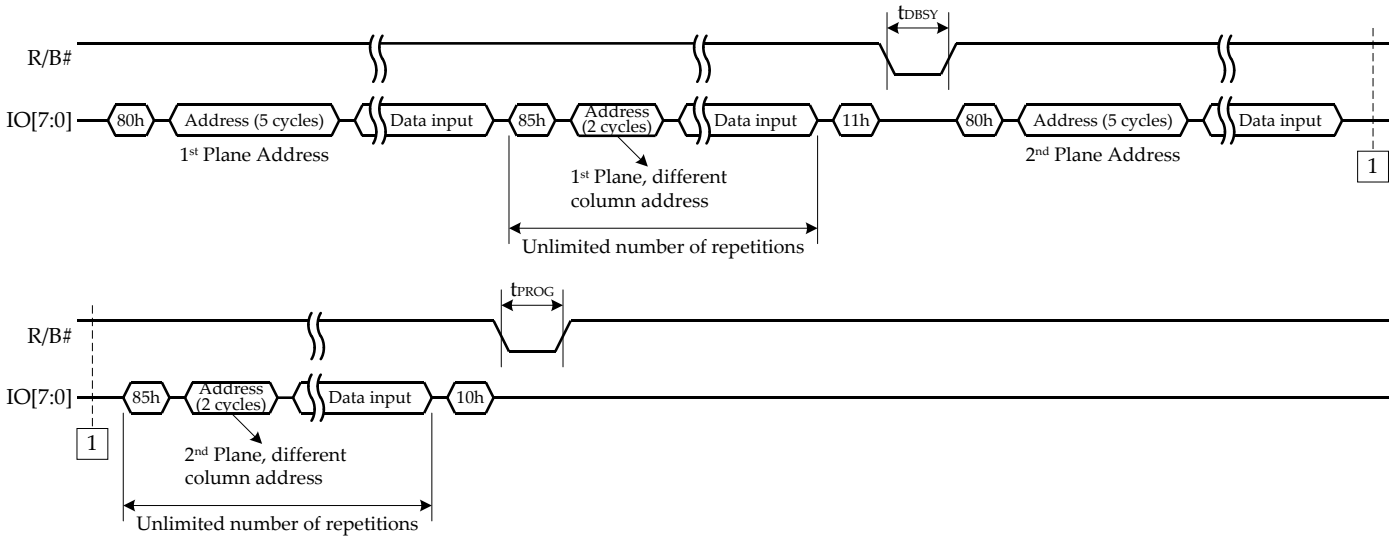

Figure 72: Two-Plane Program Page with Random Data Input

5.6. Two-Plane Program Page Cache Mode

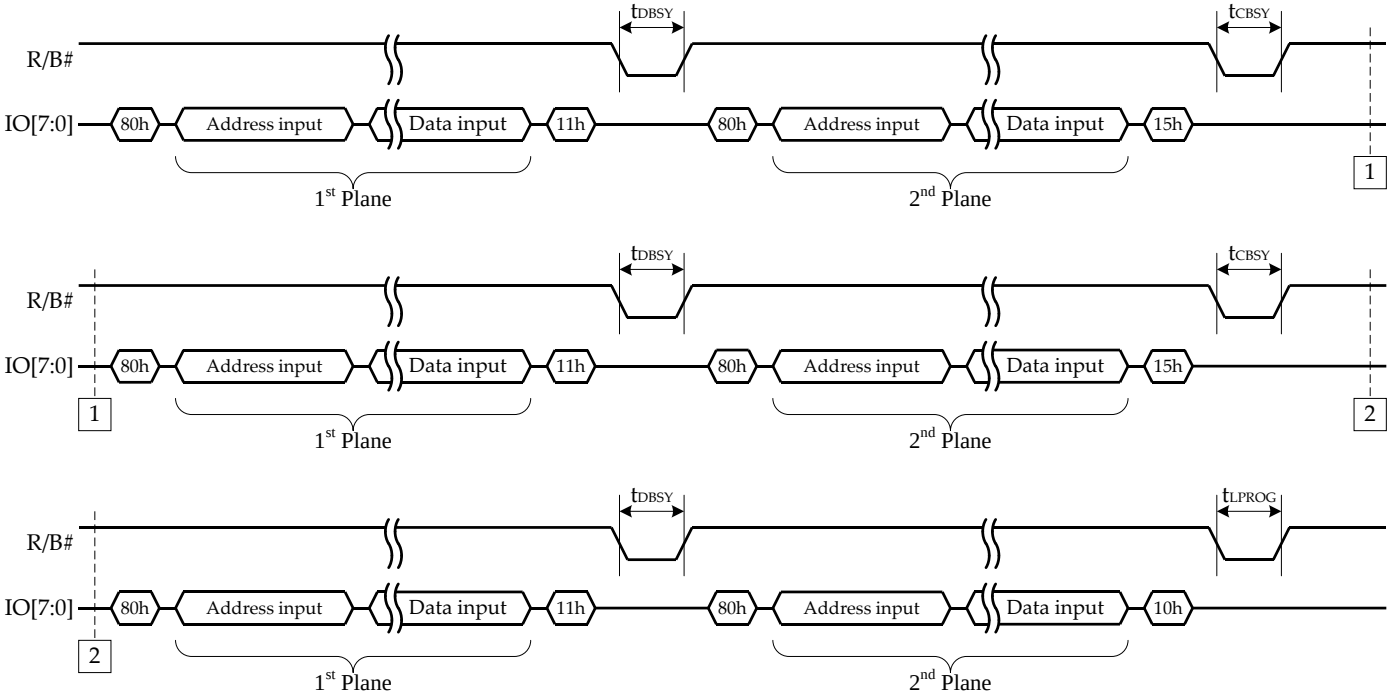

Figure 73: Two-Plane Program Page Cache Mode

5.7. Two-Plane Internal Data Move

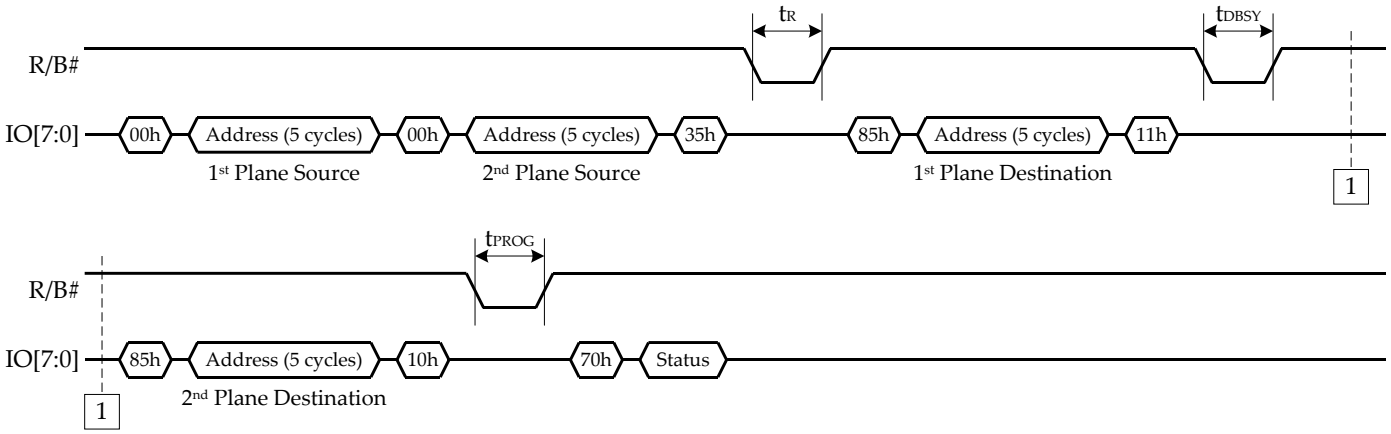

Figure 74: Two-Plane Internal Data Move

5.8. Two-Plane Internal Data Move with Two-Plane Random Data Read

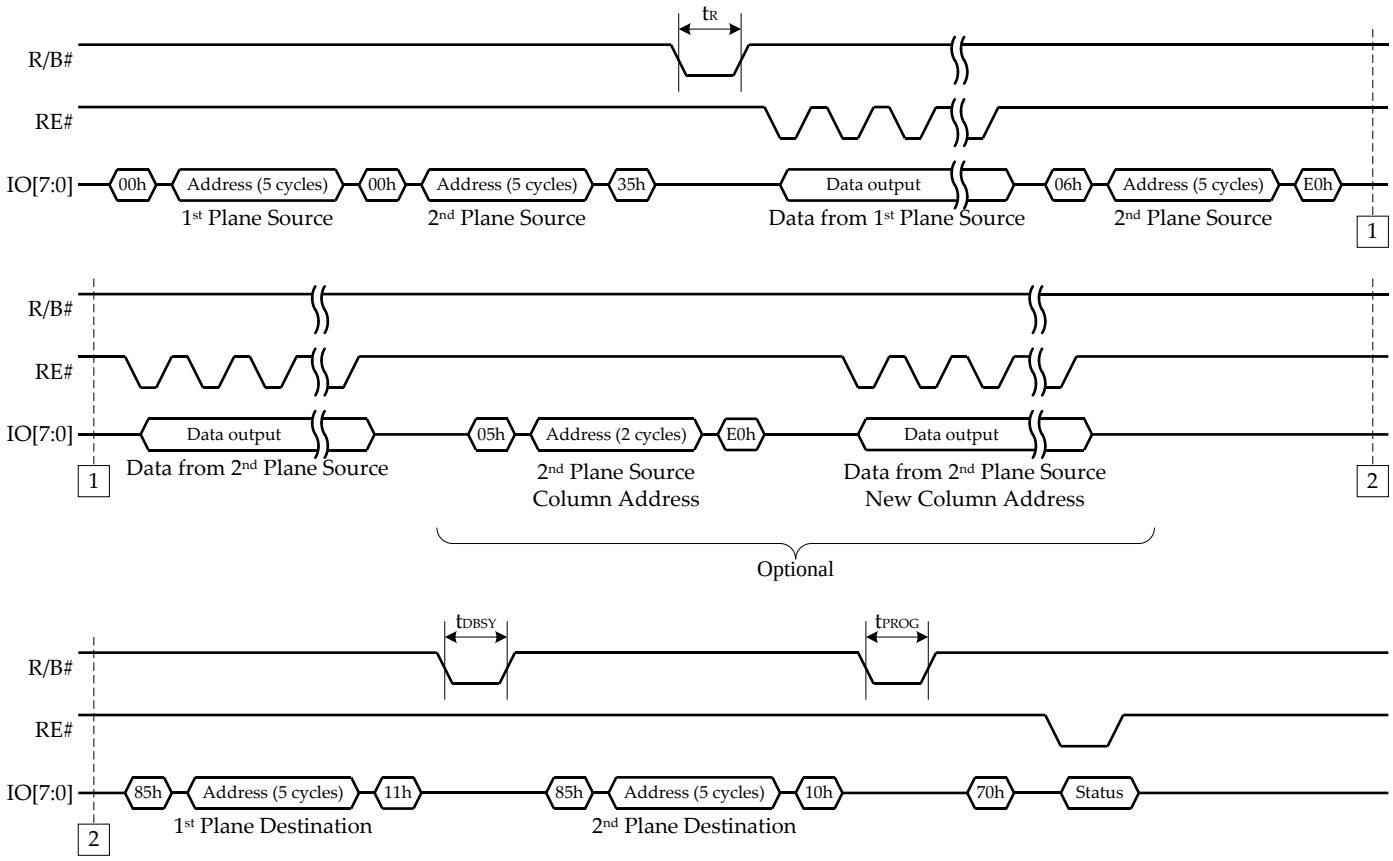

Figure 75: Two-Plane Internal Data Move with Two-Plane Random Data Read

5.9. Two-Plane Internal Data Move with Random Data Input

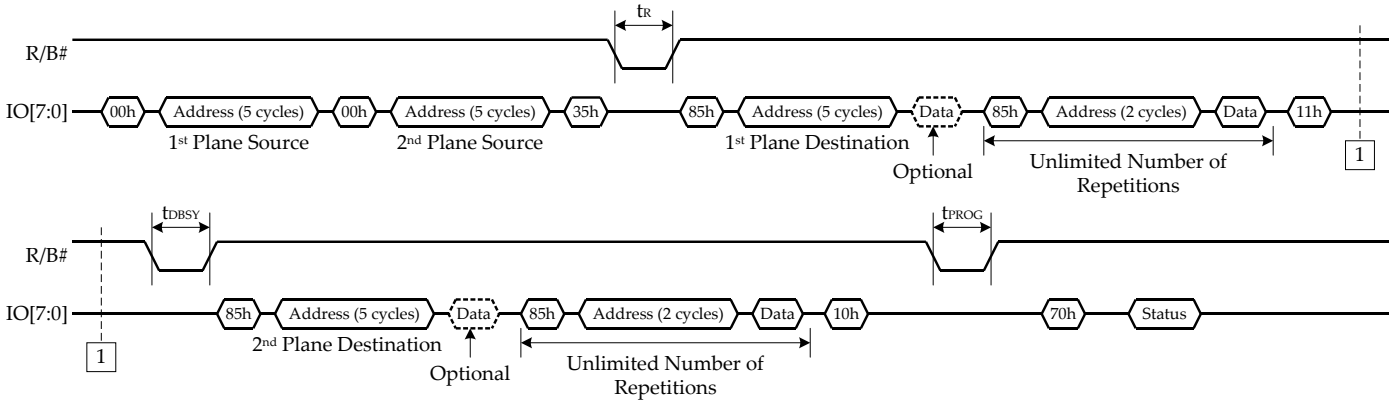

Figure 76: Two-Plane Internal Data Move with Random Data Input

5.10. Two-Plane Block Erase

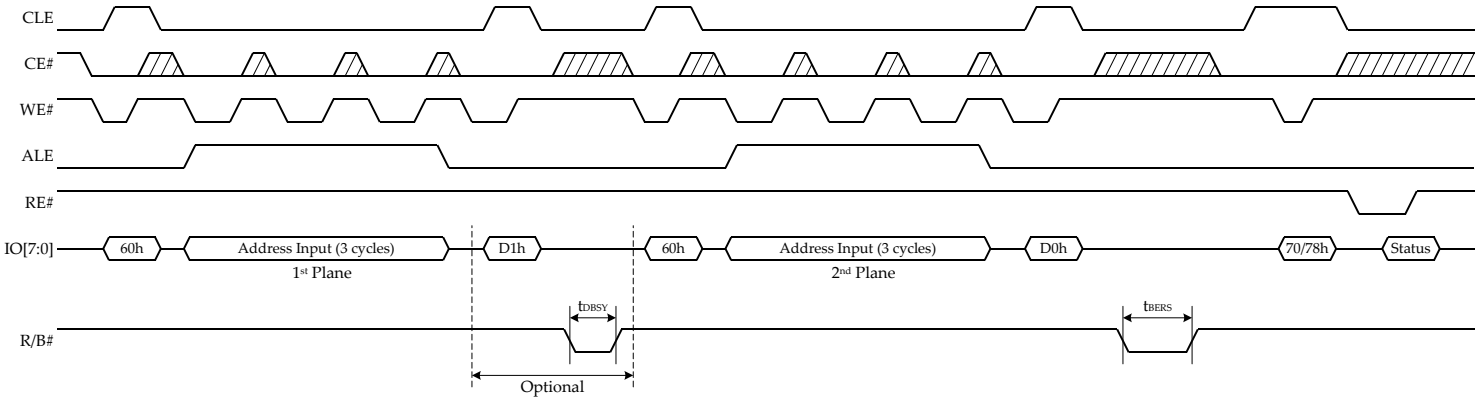

Figure 77: Two-Plane Block Erase

5.11. Two-Plane/Multiple-Die Read Status Cycle

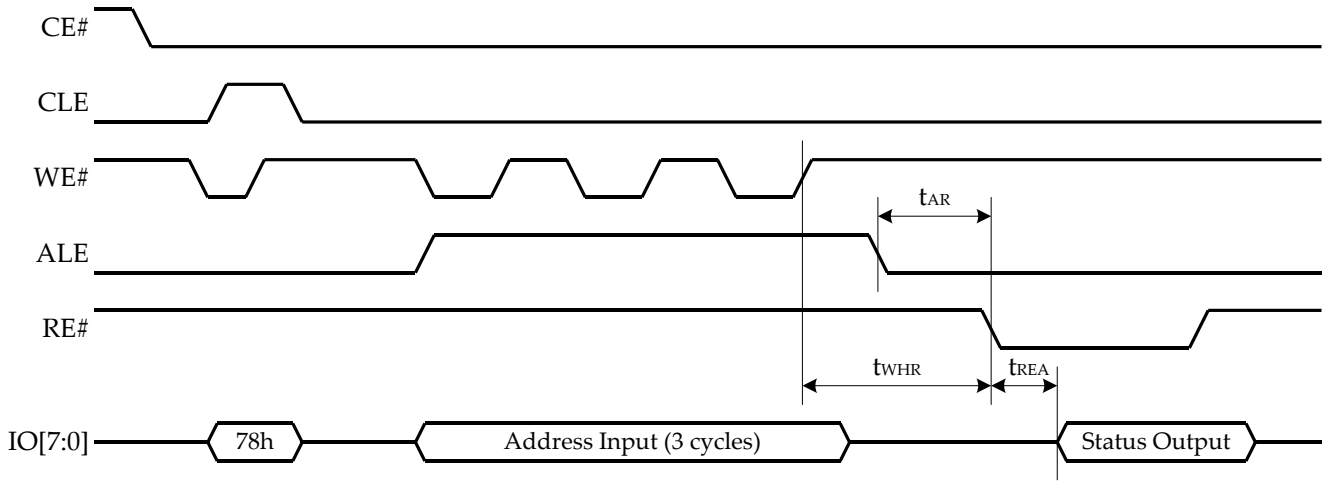

Figure 78: Two-Plane / Multiple-Die Read Status Cycle

6. Interleaved Die (Multi-LUN) Operations

For devices with more than one die (LUN) per target, system performance can be improved by interleaving operations between the dies (LUNs), which issues command to an idle die (LUN) (RDY=1) while another die (LUN) is still busy (RDY=0). Commands that allow interleaved die operation are summarized in "2.6 Command Set". After Reset (FFh), Identification (90h, ECh, EDh) and Configuration (EEh, EFh) commands, interleaved die (multi-LUN) operations are acceptable only after ARDY=1 for all LUNs on the target.

6.1. Interleaved Die (Multi-LUN) Operation Completion

While an interleaved die (multi-LUN) operation is in progress, the host may determine the completion of the operation by polling the R/B# pin, which is Low when any die (LUN) is busy and released to High when the operation is complete and all LUNs are idle.

Alternatively, the host may also use the Read Status Enhanced (78h) command to detect the status of a specific die (LUN). All operations are complete on a die when SR[5] is 1. However, the Read Status (70h) command is not prohibited during and following interleaved die (multi-LUN) operations.

6.2. Cache Operations in Interleaved Die (Multi-LUN) Operations

For cache operations like Program Page Cache (80h-15h), the die (LUN) can accept the data for another cache

operation after SR[6] becomes 1.

6.3. Program and Read in Interleaved Die (Multi-LUN) Operations

For interleaved die (multi-LUN) operations that include Program series (80h-10h, 80h-15h) and Read commands, the Program operation must be placed prior to the Read operation.
The 80h command clears the contents of the cache registers on all planes, so that the data output cycles of such Read operation must be positioned before the next Program operation.

7. Error Management

7.1. Bad Block

An invalid block or bad block is one that contains at least one page with more bad bits beyond the correction capability of the minimum required ECC. Bad blocks may develop over the lifetime of the device, but the total number of valid blocks per die (LUN) will not fall below NVB during the endurance life of the device.
Inside the NAND Flash device, all blocks are isolated from each other by internal circuitry, so the presence of bad blocks does not affect the operation of the rest of the memory array. With appropriate bad block management and error correction algorithms, NAND Flash devices with bad blocks can provide reliable data storage.
When shipped from the factory, the first block (physical block address 00h) of each CE# is guaranteed to be valid with ECC.

7.2. Factory Bad Blocks

NAND Flash devices are shipped from factory with all locations inside valid blocks erased to FFh. The device may contain invalid blocks upon delivery. These bad blocks are identified before shipping by attempting to program bad block marks at every location in the first page of each bad block, and the first spare area location in a bad block is guaranteed to contain the bad block mark. Blocks marked invalid by the factory should not be erased or programed.
See the table below for details.

Table 19: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	2008
Total available blocks per LUN	2048
First spare area location	x8: byte 2048 x16: word 1024
Bad-block mark	x8: 00h x16: 0000h
Minimum required ECC	4-bit ECC per 528 bytes
Minimum ECC with internal ECC enabled	4-bit ECC per 516 bytes (user data) + 8 bytes (parity data)
Minimum required ECC for block 0 if Program / Erase cycles are less than 1000	1-bit ECC per 528 bytes

7.3. Bad Block Management

In order to guarantee reliable data storage, the following requirements should be observed:

1. Always check the status after Program or Erase operations.
2. Use minimum required ECC in typical applications.
3. Use appropriate bad block management and wear-leveling algorithms.

8. Internal ECC and Spare Area Mapping for ECC

The NAND Flash has built-in ECC mechanism that enables 5-bit detection and 4-bit error correction in 512 bytes (x8) or 256 words (x16) of the main area and 4 bytes (x8) or 2 words (x16) of metadata I in the spare area.
Metadata II which includes two bytes (x8) or one word (x16), is not protected by ECC.
For Program operations, internal ECC circuitry generates parity bits during the busy time. For Read operations, internal ECC result is reflected in the status register; after Read operation is complete, the host should poll the status register for SR[0] to determine whether an error beyond internal ECC capability is encountered.
After Read Status command, a 00h command should be issued to return the device back to read mode.
Limitations of internal ECC include spare area (see tables below) and ECC parity areas that cannot be written to.
Each ECC user area (referred to as main and spare) should be written within one partial-page program, so that proper ECC parity can be calculated.

Table 20: Spare Area Mapping (x8)

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data
3FFh	200h	Yes	Main 1	User data
5FFh	400h	Yes	Main 2	User data
7FFh	600h	Yes	Main 3	User data
801h	800h	No		Reserved
803h	802h	No		User metadata II
807h	804h	Yes	Spare 0	User metadata I
80Fh	808h	Yes	Spare 0	ECC for main/spare 0
811h	810h	No		Reserved
813h	812h	No		User metadata II
817h	814h	Yes	Spare 1	User metadata I
81Fh	818h	Yes	Spare 1	ECC for main/spare 1
821h	820h	No		Reserved
823h	822h	No		User metadata II
827h	824h	Yes	Spare 2	User metadata I
82Fh	828h	Yes	Spare 2	ECC for main/spare 2
831h	830h	No		User data
833h	832h	No		User metadata II
837h	834h	Yes	Spare 3	User metadata I
83Fh	838h	Yes	Spare 3	ECC for main/spare 3

Bad Block Information	ECC Parity	User Data (Metadata)
2 bytes	8 bytes	6 bytes

9. Electrical Specifications

Table 21: Absolute Maximum Ratings

Parameter / Condition		Symbol	Min	Max	Unit
Voltage input	1.8V	V_{IN}	-0.6	2.4	V
	3.3V		-0.6	4.6	V
V_{CC} supply voltage	1.8V	V_{CC}	-0.6	2.4	V
	3.3V		-0.6	4.6	V
Storage temperature		T_{STG}	-65	150	°C
Short circuit output current, I/Os		-	-	5	mA

Notes:

1. Stresses greater than those listed in this table may cause permanent damage to the device.
2. This is stress rating only. Device functional operation at these conditions is not guaranteed.
3. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 22: Recommended Operating Conditions

Parameter / Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	-	70	°C
	Industrial		-40	-	85	°C
	Automotive Industrial Grade		-40	-	85	°C
	Automotive Grade		-40	-	105	°C
V_{CC} supply voltage	1.8V	V_{CC}	1.7	1.8	1.95	V
	3.3V		2.7	3.3	3.6	V
Ground supply voltage		V_{SS}	0	0	0	V

Table 23: Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit
Valid block number	NVB	NM9A02G08AFI	2008	2048	Blocks

Notes:

1. The total number of valid blocks will not drop below NVB during the endurance of the device.
2. Block 00h is guaranteed to be valid with ECC when shipped from the factory.

Table 24: Capacitance

Description	Symbol	Max	Unit
Input capacitance	C_{IN}	10	pF
Input/output capacitance (I/O)	C_{IO}	10	pF

Notes:

1. These parameters are verified in device characterization and are not 100% tested.
2. Test condition: T_C = 25°C; f = 1MHz; Vin = 0V.

Table 25: Test Conditions

Parameter		Value	Notes
Input pulse levels		0.0V to V_{CC}	
Input rise and fall times	1.8V	2.5ns	
	3.3V	5.0ns	
Input and output timing levels		V_{CC}/2	
Output load		1 TTL GATE and CL = 30pF (1.8V)	1
		1 TTL GATE and CL = 50pF (3.3V)	
Output load		1 TTL GATE and CL = 30pF (1.8V)	1
		1 TTL GATE and CL = 50pF (3.3V)	

Notes:

1. The parameter is verified in device characterization and is not 100% tested.

9.1. DC Characters and Operating Conditions

Table 26: DC Characteristics and Operating Conditions (3.3V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes

Sequential Read current	tRC = tRC (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	-	25	35	mA	
Program current	-	I_{CC2}	-	25	35	mA	
Erase current	-	I_{CC3}	-	25	35	mA	
Standby current (TTL)	CE# = V_{IH}; WP# = 0V/V_{CC}	I_{SB1}	-	-	1	mA	1
Standby current (CMOS)	CE# = V_{CC} - 0.2V; WP# = 0V/V_{CC}	I_{SB2}	-	20	100	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	-	-	10 per die	mA	2
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	-	-	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	-	-	±10	µA	
Input high voltage	IO[7:0], IO[15:0], CE#, CLE, ALE, WE#, RE#, WP#	V_{IH}	0.8 x V_{CC}	-	V_{CC}+ 0.3	V	
Input low voltage, all inputs	-	V_{IL}	-0.3	-	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –400µA	V_{OH}	0.67 x V_{CC}	-	-	V	3
Output low voltage	I_{OL} = 2.1mA	V_{OL}	-	-	0.4	V	3
Output low current	V_{OL} = 0.4V	I_{OL}(R/B#)	8	10	-	mA	4

Notes:

1. I_{SB1} is 15mA at operating temperature 105°C.
2. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches V_{CC}(MIN).
3. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to full.
4. I_{OL}(R/B#) may need to be relaxed if R/B pull-down strength is not set to full.

Table 27: DC Characteristics and Operating Conditions (1.8V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential Read current	tRC = tRC (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	-	13	20	mA	1, 2
Program current	-	I_{CC2}	-	10	20	mA	1, 2
Erase current	-	I_{CC3}	-	10	20	mA	1, 2
Standby current (TTL)	CE# = V_{IH}; WP# = 0V/V_{CC}	I_{SB1}	-	-	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; WP# = 0V/V_{CC}	I_{SB2}	-	10	50	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	-	-	10 per die	mA	3
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	-	-	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	-	-	±10	µA	

Input high voltage	IO[7:0], IO[15:0], CE#, CLE, ALE, WE#, RE#, WP#	V_{IH}	0.8 x V_{CC}	-	V_{CC}+ 0.3	V	
Input low voltage, all inputs	-	V_{IL}	-0.3	-	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = -100µA	V_{OH}	V_{CC} - 0.1	-	-	V	4
Output low voltage	I_{OL} = +100µA	V_{OL}	-	-	0.1	V	4
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL}(R/B#)	3	4	-	mA	5

Notes:

1. Typical and maximum values are for single-plane operation only. If device supports dual-plane operation, values are 20mA (TYP) and 40mA (MAX).
2. Values are for single-die operations. Values could be higher for interleaved-die operations.
3. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches V_{CC}(MIN).
4. Test conditions for V_{OH} and V_{OL}.
5. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full.

9.2. AC Characteristics

9.2.1.Command, Data and Address Input

Table 28: AC Characteristics: Command, Data and Address Input (3.3V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	tADL	70	-	ns	1, 2
ALE hold time	tALH	5	-	ns	1
ALE setup time	tALS	10	-	ns	1
CE# hold time	tCH	5	-	ns	1
CLE hold time	tCLH	5	-	ns	1
CLE setup time	tCLS	10	-	ns	1
CE# setup time	tCS	15	-	ns	1
Data hold time	tDH	5	-	ns	1
Data setup time	tDS	7	-	ns	1
Write cycle time	tWC	20	-	ns	1, 2
WE# pulse width High	tWH	7	-	ns	1, 2
WE# pulse width	tWP	10	-	ns	1, 2
WP# transition to WE# Low	tWW	100	-	ns	1

Notes:

1. Operating mode timings meet ONFI timing mode 5 parameters.
2. Timing for tADL begins in the address cycle on the final rising edge of WE#, and ends at the first rising edge of WE# in data input.

Table 29: AC Characteristics: Command, Data and Address Input (1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	tADL	70	-	ns	1, 2
ALE hold time	tALH	5	-	ns	1
ALE setup time	tALS	10	-	ns	1
CE# hold time	tCH	5	-	ns	1

CLE hold time	tCLH	5	-	ns	1
CLE setup time	tCLS	10	-	ns	1
CE# setup time	tCS	20	-	ns	1
Data hold time	tDH	5	-	ns	1
Data setup time	tDS	10	-	ns	1
Write cycle time	tWC	25	-	ns	1, 2
WE# pulse width High	tWH	10	-	ns	1, 2
WE# pulse width	tWP	12	-	ns	1, 2
WP# transition to WE# Low	tWW	100	-	ns	1

Notes:

1. Operating mode timings meet ONFI timing mode 4 parameters.
2. Timing for tADL begins in the address cycle on the final rising edge of WE#, and ends at the first rising edge of WE# in data input.

9.2.2.Normal Operation

Table 30: AC Characteristics: Normal Operation (3.3V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	tAR	10	-	ns	1
CE# access time	tCEA	-	25	ns	1
CE# High to output High-Z	tCHZ	-	50	ns	1, 2
CLE to RE# delay	tCLR	10	-	ns	1
CE# HIGH to output hold	tCOH	15	-	ns	1
Output High-Z to RE# Low	tIR	0	-	ns	1
Read cycle time	tRC	20	-	ns	1
RE# access time	tREA	-	16	ns	1
RE# High hold time	tREH	7	-	ns	1
RE# High to output hold	tRHOH	15	-	ns	1
RE# High to WE# Low	tRHW	100	-	ns	1
RE# High to output High-Z	tRHZ	-	100	ns	1, 2
RE# Low to output hold	tRLOH	5	-	ns	1
RE# pulse width	tRP	10	-	ns	1
Ready to RE# Low	tRR	20	-	ns	1
Reset time (Read/Program/Erase)	tRST	-	5/10/500	µs	1, 3
WE# High to busy	tWB	-	100	ns	1
WE# High to RE# Low	tWHR	60	-	ns	1

Notes:

1. AC characteristics may need to be relaxed if I/O drive strength is not set to full.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
3. For the first time the Reset (FFh) command is issued while the device is idle, the device goes busy for a maximum of 1ms. Thereafter, the device goes busy for a maximum of 5µs.

Table 31: AC Characteristics: Normal Operation (1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	tAR	10	-	ns	1
CE# access time	tCEA	-	25	ns	1

CE# High to output High-Z	tCHZ	-	50	ns	1, 2
CLE to RE# delay	tCLR	10	-	ns	1
CE# HIGH to output hold	tCOH	15	-	ns	1
Output High-Z to RE# Low	tIR	0	-	ns	1
Read cycle time	tRC	25	-	ns	1
RE# access time	tREA	-	22	ns	1
RE# High hold time	tREH	10	-	ns	1
RE# High to output hold	tRHOH	15	-	ns	1
RE# High to WE# Low	tRHW	100	-	ns	1
RE# High to output High-Z	tRHZ	-	65	ns	1, 2
RE# Low to output hold	tRLOH	3	-	ns	1
RE# pulse width	tRP	12	-	ns	1
Ready to RE# Low	tRR	20	-	ns	1
Reset time (Read/Program/Erase)	tRST	-	5/10/500	µs	1, 3
WE# High to busy	tWB	-	100	ns	1
WE# High to RE# Low	tWHR	80	-	ns	1

Notes:

1. AC characteristics may need to be relaxed if I/O drive strength is not set to full.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
3. For the first time the Reset (FFh) command is issued while the device is idle, the device goes busy for a maximum of 1ms. Thereafter, the device is busy for a maximum of 5µs.

9.3. Program/Erase Characteristics

Table 32: Program/Erase Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial-page programs	NOP	-	4	cycles	1
BLOCK ERASE operation time	tBERS	0.7	3	ms	
Busy time for Program Cache operation	tCBSY	3	600	µs	2
Cache read busy time	tRCBSY	3	25	µs	
Busy time for Set Features and Get Features operations	tFEAT	-	1	µs	
Busy time for OTP Data Program operation if OTP is protected	tOBSY	-	30	µs	
Busy time for Program/Erase on locked blocks	tLBSY	-	3	µs	
Program Page operation time, internal ECC disabled	tPROG	200	600	µs	8
Program Page operation time, internal ECC enabled	tPROG_ECC	220	600	µs	3, 8
Data transfer from Flash array to data register, internal ECC disabled	tR	-	25	µs	6, 7
Data transfer from Flash array to data register, internal ECC enabled	tR_ECC	45	70	µs	3, 5
Busy time for OTP Data Program operation if OTP is protected, internal ECC enabled	tOBSY_ECC	-	50	µs	

Busy time for Two-Plane Program Page or Two-Plane Block Erase operation	tDBSY	0.5	1	μs	

Notes:

1. Four total partial-page programs to the same page. If ECC is enabled, then the device is limited to one partial-page program per ECC user area, not exceeding four partial-page programs per page.
2. tCBSY MAX time depends on timing between internal program completion and data-in.
3. Parameters are with internal ECC enabled.
4. Typical is nominal voltage and room temperature.
5. Typical tR_ECC is under typical process corner, nominal voltage, and at room temperature.
6. Data transfer from Flash array to data register with internal ECC disabled.
7. AC characteristics may need to be relaxed if I/O drive strength is not set to full.
8. Typical program time is defined as the time within which more than 50% of the pages are programmed at nominal voltage and room temperature.

10. Part Numbering

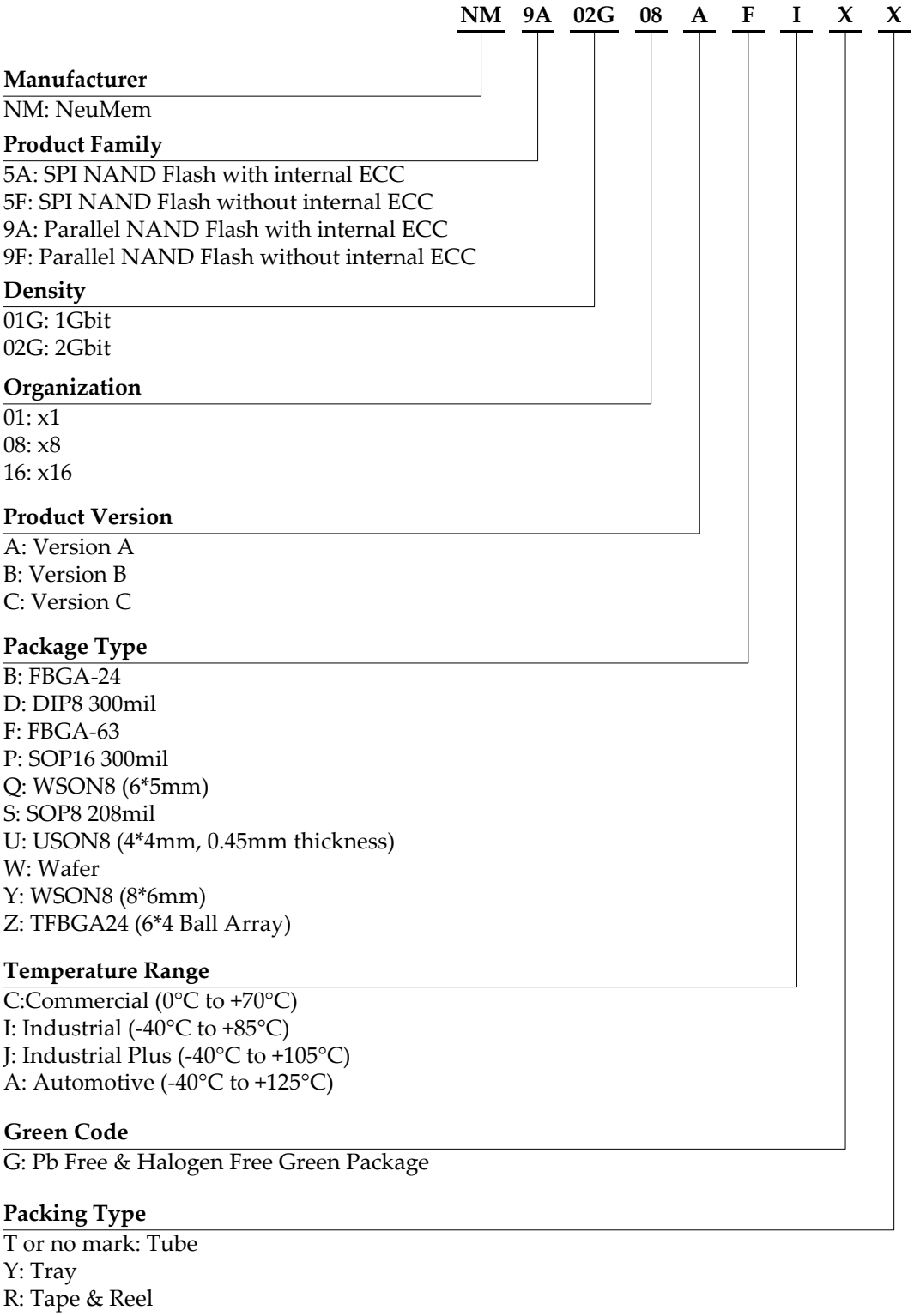

Figure 79: Part Numbering Information

11. Package Information

11.1. Signal Assignments

The NM9A02G08 device is offered in a number of pin configurations.

11.1.1. 48-Pin TSOP

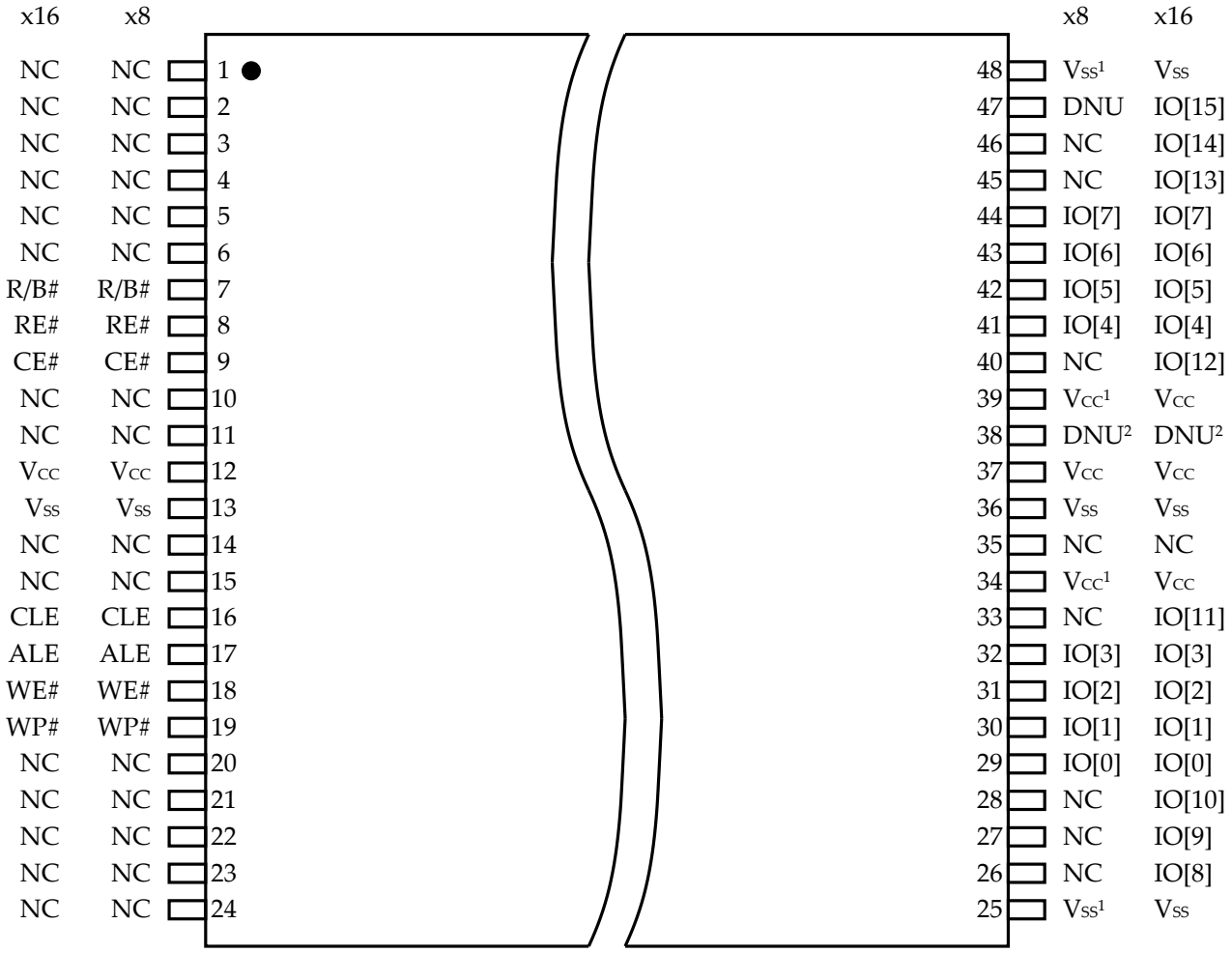

Figure 80: 48-Pin TSOP – Type 1, CPL (Top View)

Notes:

1. These pins might not be bonded in the package; however, NeuMem recommends that the customer connect these pins to the designated external sources for ONFI compatibility.
2. For 3V devices, pin 38 is DNU; for 1.8V devices, pin 38 is LOCK.

11.1.2. 63-Ball VFBGA, x8

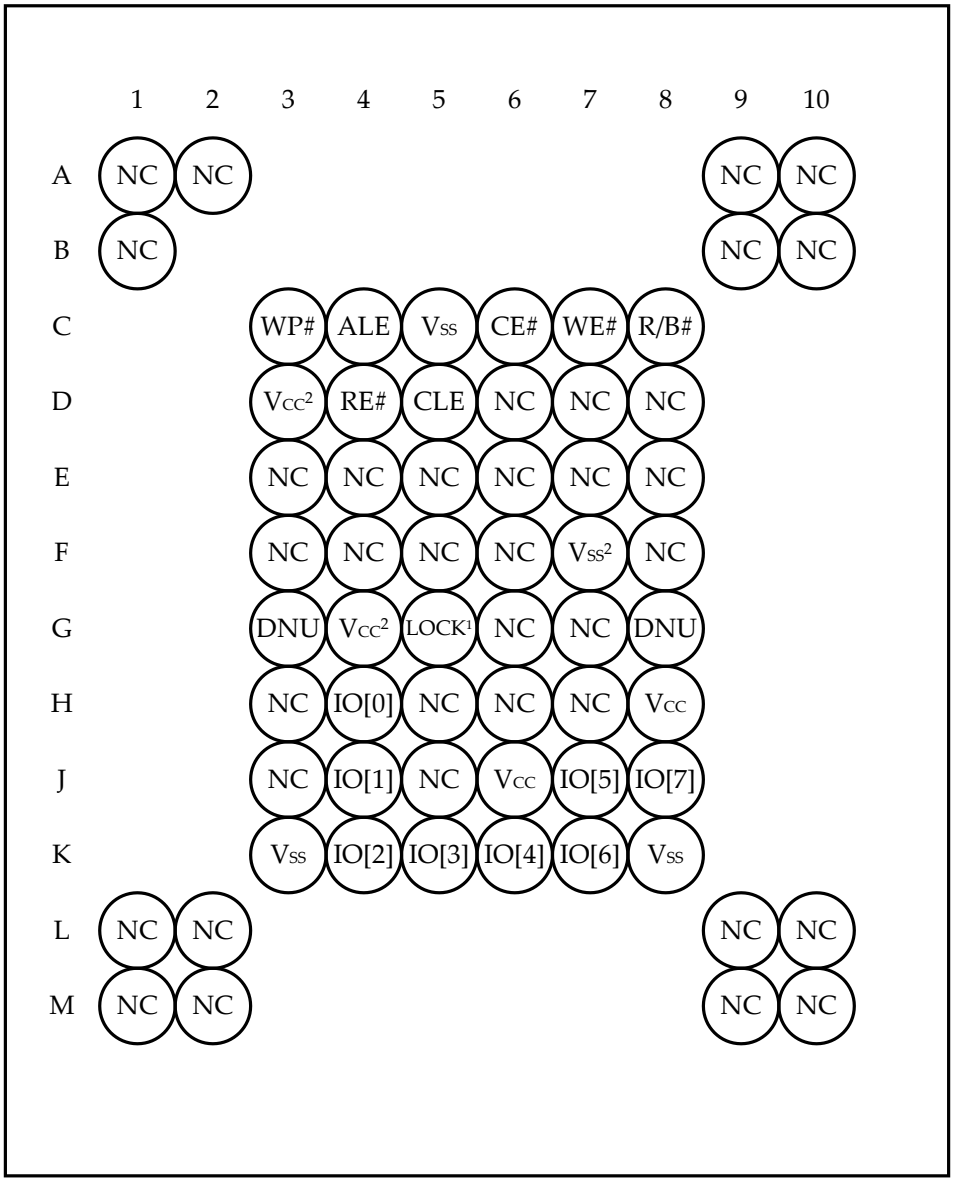

Figure 81: 63-Ball VFBGA, x8 (Balls Down, Top View)

Notes:

1. For 3V devices, G5 changes to DNU. No LOCK function is available on 3.3V devices.
2. These pins might not be bonded in the package; however, NeuMem recommends that the customer connect these pins to the designated external sources for ONFI compatibility.

11.1.3. 63-Ball VFBGA, x16

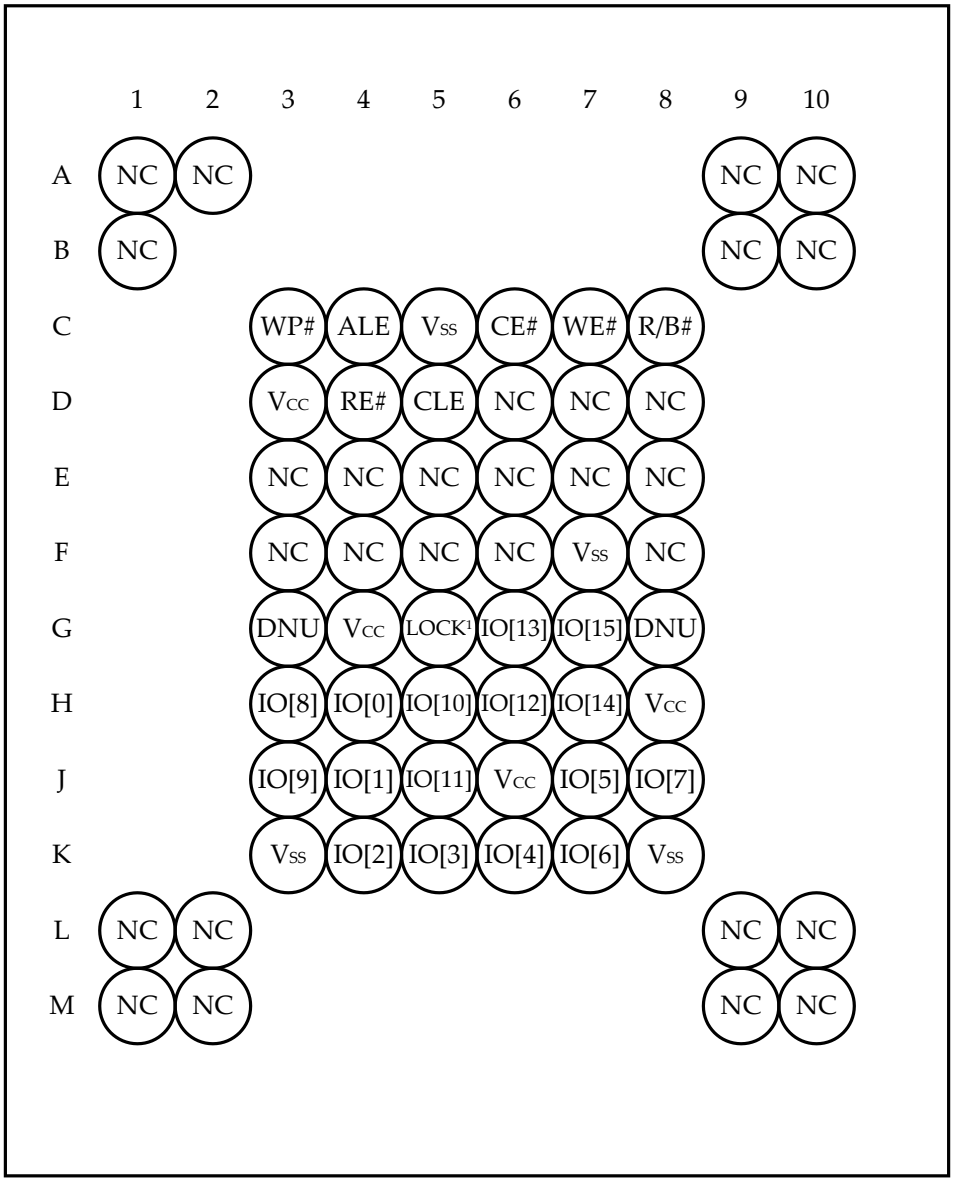

Figure 82: 63-Ball VFBGA, x16 (Balls Down, Top View)

Notes:

1. For 3V devices, G5 changes to DNU. No LOCK function is available on 3.3V devices.

11.2. Package Dimensions

11.2.1. 48-Pin TSOP

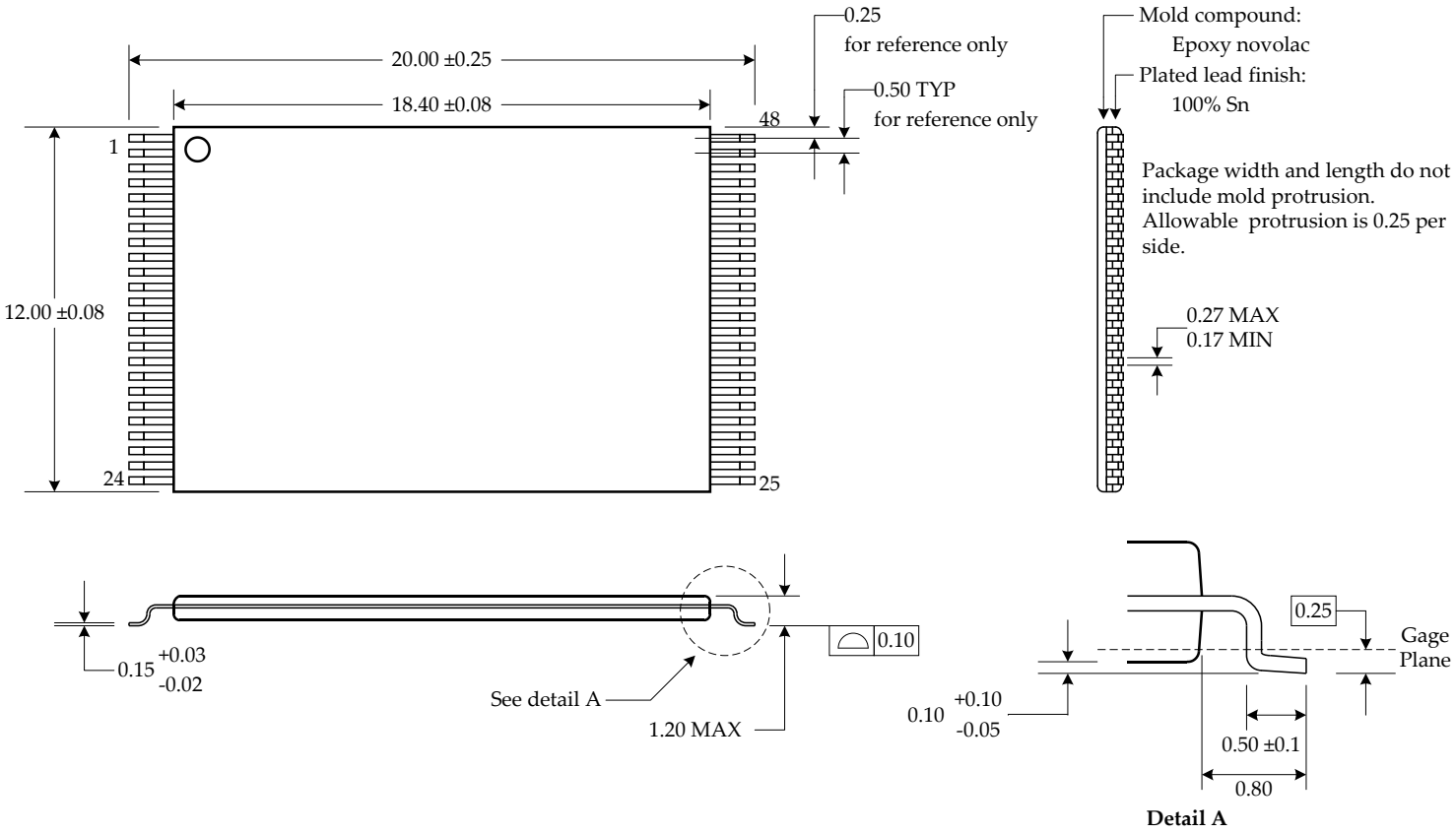

Figure 83: 48-Pin TSOP – Type 1, CPL

Notes:

1. All dimensions are in millimeters.

11.2.2. 63-Ball VFBGA (10.5mm x 13mm)

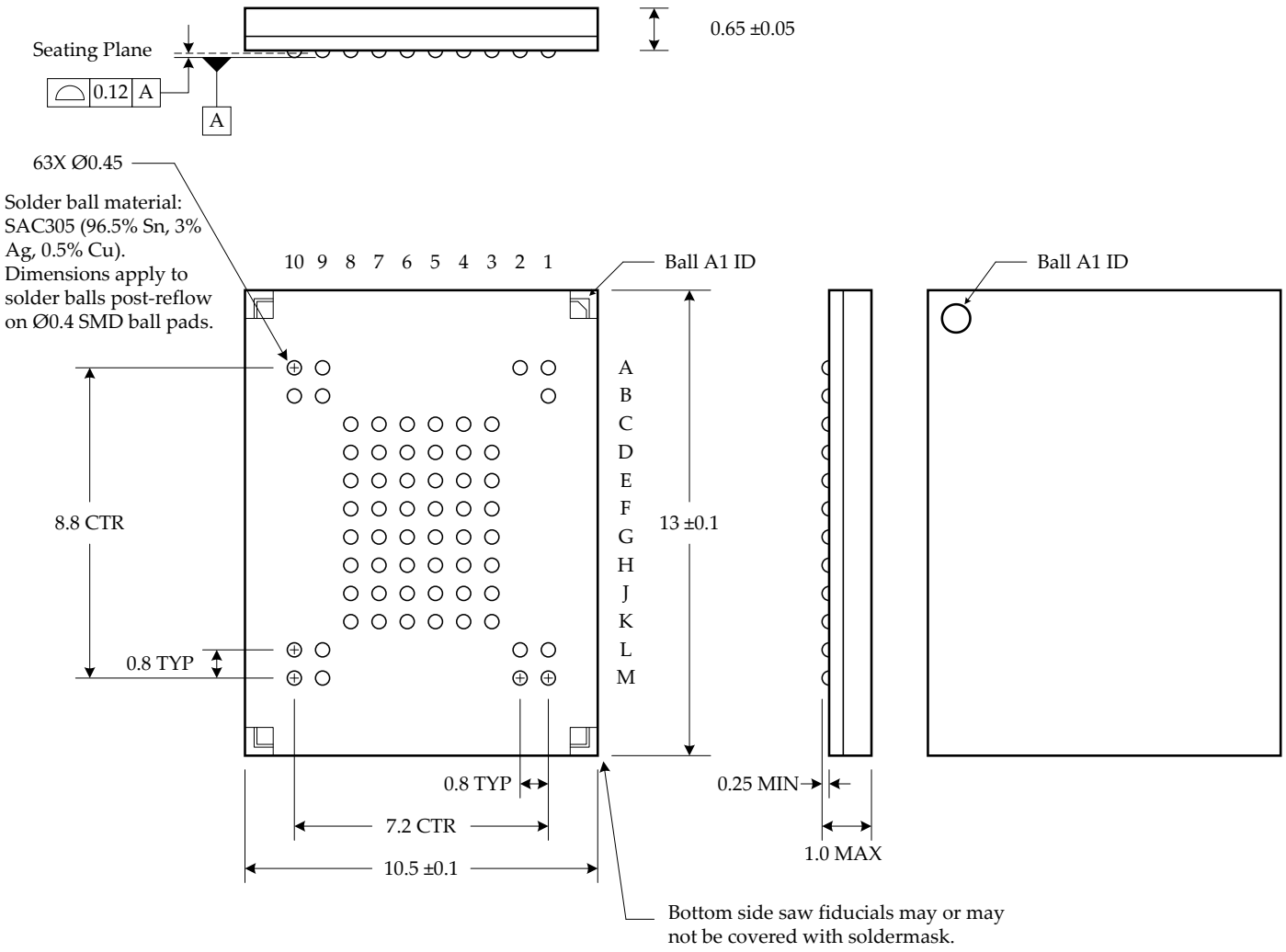

Figure 84: 63-Ball VFBGA (10.5mm x 13mm)

Notes:

1. All dimensions are in millimeters.

11.2.3. 63-Ball VFBGA (9mm x 11mm)

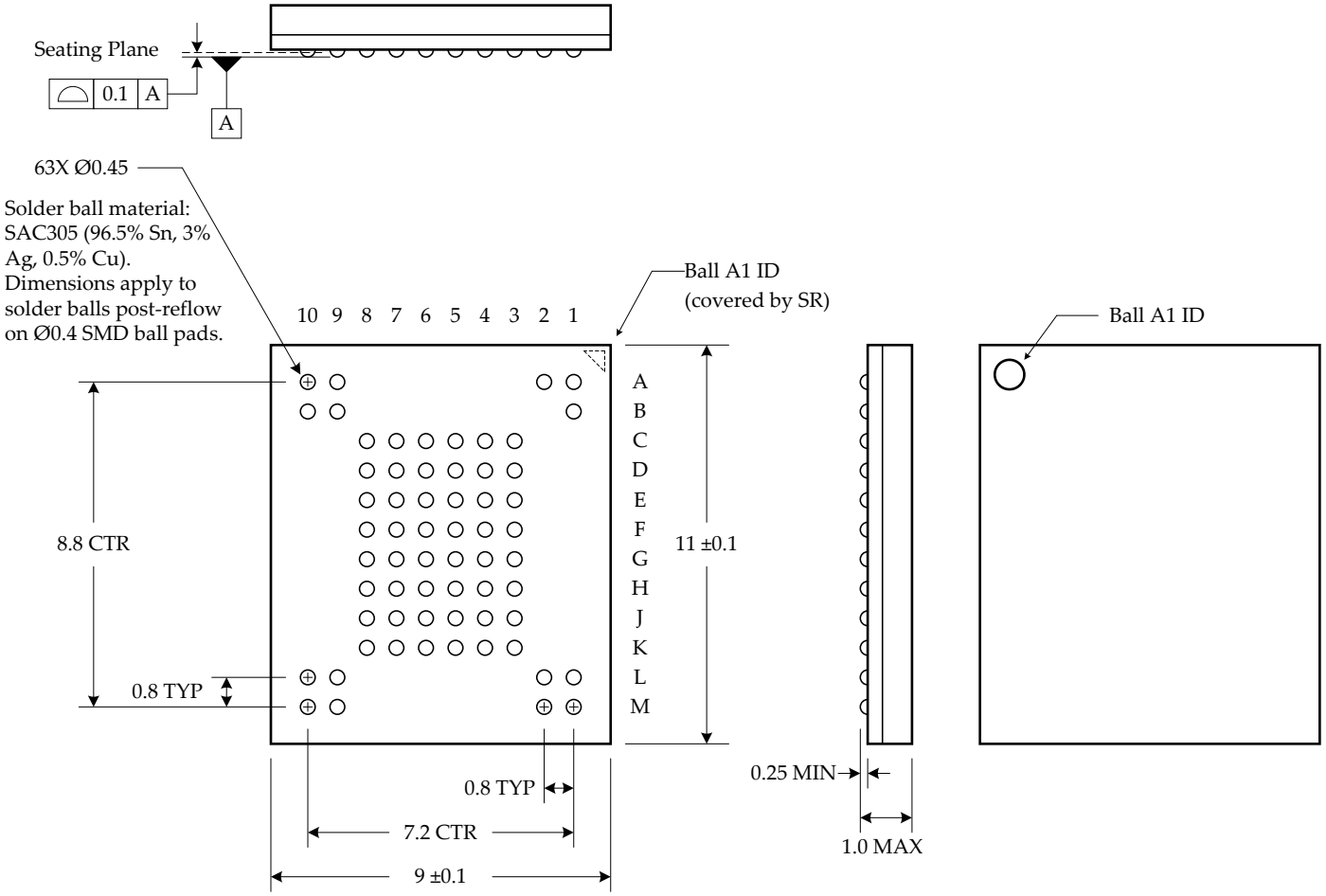

Figure 85: 63-Ball VFBGA (9mm x 11mm)

Notes:

1. All dimensions are in millimeters.

12. Revision History

The table below shows the revision history of this document.

Date	Version	Revision
Oct 28, 2020	v1.0	NeuMem

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